RESPECT

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BOSCH [2] AIRBUS [3]

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Context

> Multi-cores and heterogeneous platforms are essential to provide complex critical systems from the **automotive**, **space** and **railway** markets with **cost-effective** and **power-efficient** parallel capabilities.

> The **critical embedded market** (CEM) presents several challenges regarding safety certification, causing tedious and expensive Verification & Validation (V&V) processes.

> Although high-level **parallel programming models (PPM)** are very effective at leveraging the performance of heterogeneous and parallel processor architectures, they lack features to ensure the dependability of the system in terms of **functional correctness**, **real-time** constraints, **safety** and **reliability**.

Objectives

*RESPECT will develop a complete software framework, **Dependable Parallel Environment (DePE)**, to facilitate the development of advanced critical software for parallel and heterogeneous computers by holistically addressing dependability and high-performance.*

1. Provide **enhanced PPM** and tools to ease parallelization while abstracting the complexities of the underlying architecture.
2. Develop off-line / on-line mechanisms to minimize the impact of parallel execution in terms of **overhead** and **contention**.
3. Develop off-line / on-line mechanisms to enhance **reliability** and **safety** while exploiting the parallel resources of the system.
4. Provide a **correct-by-construction** framework that allows the analyzability of the system in terms of real-time / dependability requirements and functional correctness.

Solution

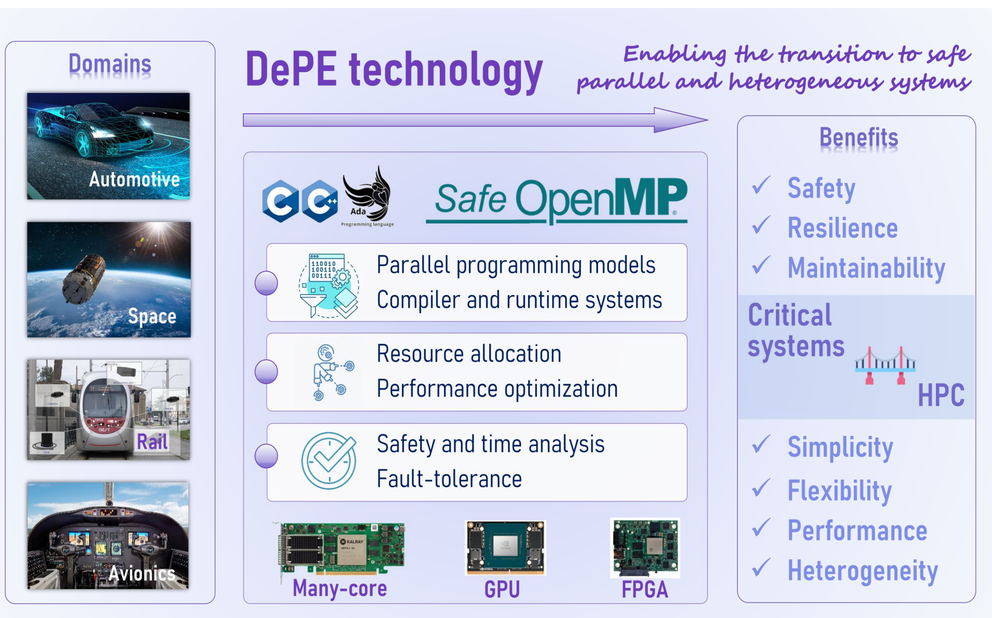
Relevant benchmarks

> **On-board Processing Benchmarks (OBPMark)**

Spacecraft applications for image and radar processing, data and image compression, signal processing and machine learning.

> **Darmstadt Automotive Parallel Heterogeneous Benchmark-Suite (DAPHNE)**

Automotive applications from the Autoware project for the evaluation of heterogeneous, parallel programming models.



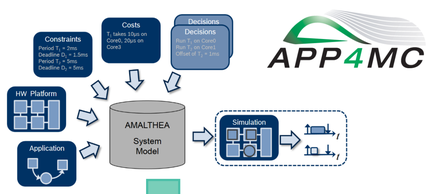
Extensions

> **The taskgraph framework**
- ✓ Represent a region of code as a Task Dependency Graph (TDG)
- ✓ Avoid the execution of user code to orchestrate tasks
- ✓ Avoid dependency resolution and task instantiation
- ✓ Enable timing analysis based on Direct Acyclic Graphs (DAG)
- ✓ Expose interoperability with CUDA graphs

> **Task-level replication**
- ✓ Temporal and spatial
- ✓ Safety architecture

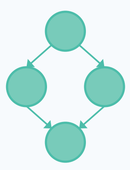
Transfer of technology

AMPERE — A Model-driven development framework for highly Parallel and EneRgy-Efficient computation supporting multi-criteria optimisation



> AMALTHEA **Domain Specific Modelling Language** (DSML)
> APP4MC **Synthetic Load Generator** (SLG) for C+OpenMP(+ROS, *Robot Operating System*)

OpenMP — LLVM COMPILER INFRASTRUCTURE



> TDG for multi-criteria analysis:
- ✓ energy models
- ✓ time predictability
- ✓ performance

PikeOS RTOS & Hypervisor — ERIKA 3

> NVIDIA Jetson Xavier AGX

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Contributions

> **Increase Technology Readiness Level to 6**

> **Consolidate the taskgraph framework**
- ✓ *Introduction of a taskgraph directive in the OpenMP specification*
- ✓ *Upload to LLVM upstream taskgraph extensions for dynamic recording*
- ✓ *Introduce in LLVM static analysis for static partial taskgraph discovery*

> **Extend and test features for resilience**
- ✓ *Task-level replication*
- ✓ *Fault-recovery with coarse-grained checkpointing*

> **Consolidate and extend application domains:**
- ✓ *Automotive (Bosch)*
- ✓ *(new) Space (Airbus)*
- ✓ *(new) Avionics (Collins Aerospace)*

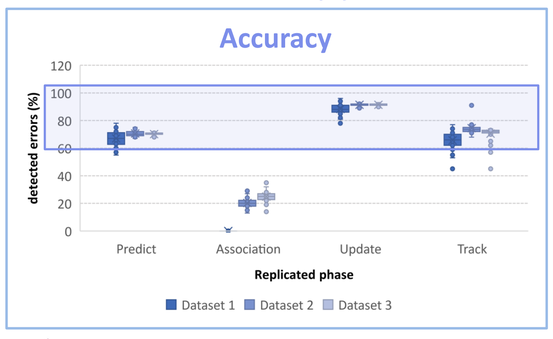
RESPECT

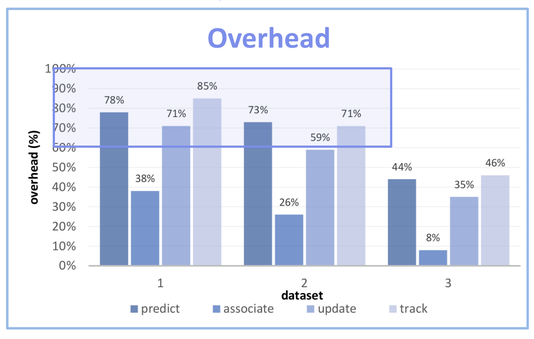
Timeline and Tasks

Phase 1	**System modelling**	
	System model description	✓
	Board selection and set up	✓
	Safety requirements	✓
	Use case preparation	✓
Phase 2	**DePE technology**	
	PPM	
	LLVM adaptations	
	Evaluation	
Phases 1 and 2	**Management**	
	Dissemination	
	Exploitation	
	Roadmap certification	

Preliminary results

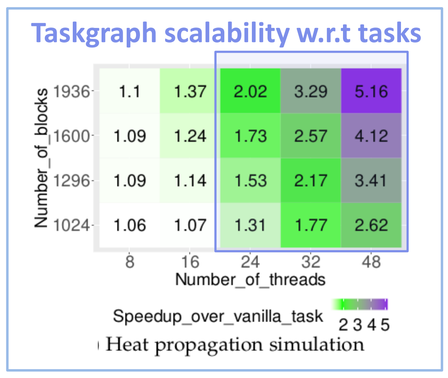
> **Task-level parallel replication**
- ✓ *Application: Obstacle Detection and Avoidance System (from THALES)*
- ✓ *Replication design: Phases: predict, association, update, and track*
  Datasets: (1) scattered, (2) crowded, (3) inflated
- ✓ *Hardware: NVIDIA Jetson Xavier AGX*
- ✓ *Fault model: 1 bit flip per run in a relevant variable of a replicated task*

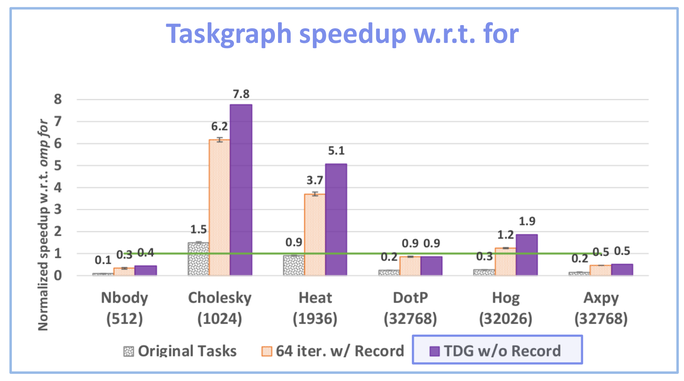




Boosting productivity and resiliency through automated software replication. AUJ 43(3)

> **Fine grained predictable parallelism**
- ✓ *Applications: NAS parallel benchmarks, heat propagation, gravity force, axpy, dot-product, Cholesky factorization, object detector based on histogram of gradients*
- ✓ *Parallelization approaches: Tasks/Taskloops and For loops*
- ✓ *Hardware: 24x dual-socket Intel Xeon Platinum*





Taskgraph: A Low Contention OpenMP Tasking Framework. C. Yu, et al. arXiv:2212.04771

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