A Model-driven development framework for highly Parallel and EneRgy-Efficient computation supporting multi-criteria optimisation

D7.7 Final Exploitation Report

Version 1.0

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V1.0	Final version

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Executive Summary

The European project AMPERE developed a full ecosystem supporting and easing the development of future high-performance and real-time embedded applications that require the non-functional requirements (such as time predictability, energy-efficiency, safety and security) inherited from the cyber-physical interactions, on heterogeneous architecture including multi-core, GPU and FPGA acceleration.

The objective of this project was to use the most advanced energy-efficient and highly-parallel heterogeneous platforms to fully exploit the benefits of performance demanding emerging technologies, such as artificial intelligence or big data analytics. To reach such goal, AMPERE has used a combination of model-driven engineering (MDE) and parallel execution, two important technical challenges at the system design and the computing software stack of CPS.

The AMPERE project targeted TRLs 2-5 and delivers a working prototype tested in two different use cases described in the deliverable D1.1 “System models requirement and use case selection” (Intelligent Predictive Cruise Control and Obstacle Detection and Avoidance System). The AMPERE prototype exploited the heterogenous platforms selected by partners in the deliverable D5.1 “Reference parallel heterogeneous hardware selection” (i.e. Xilinx UltraScale+ MPSoC and NVIDIA Jetson AGX Xavier), demonstrating improvement over the state of the art in industrial and professional domains.

This is the final exploitation report of AMPERE Work Package 7. Where applicable, it updates market analyses and individual exploitation plans, and in preparation of future work on joint exploitation, identifies exploitable assets provided by AMPERE.

1. Introduction

Exploitation is a major commitment for AMPERE as proven by the diversity of industries in the consortium. The exploitation activities include the AMPERE ecosystem and the tools that form it and the definition of a roadmap for the adoption of parallel heterogeneous computing in safety critical systems. The fact that the AMPERE ecosystem is based on already existing tools (most of them owned by AMPERE partners) targeting COTS parallel heterogeneous computing platforms, provides two key exploitation advantages:

- The time-to-market will be reduced as most of these tools are already used in industry.
- It will enable partners to incorporate into their portfolio offerings tools supporting COTS low-energy parallel heterogeneous computing platforms, potentially increasing their revenues.

In the scope of the task 7.2 “Exploitation activities” of WP7, three exploitation reports are delivered at each milestone as shown in Table 1. Previously D7.3 has described our initial plans for the exploitation of the technologies and covers the first 12 months of activities carried out in the Task 7.2. Then, D7.5 described our intermediate plans for the exploitation of the technologies and covers the second 12 months of activities carried out in the Task 7.2. This deliverable, D7.7, describes our intermediate plans for the exploitation of the technologies and covers the third 12 months of activities carried out in the Task 7.2.

Table 1. Exploitation reports

Deliverable	Deliverable Name	Deliverable Date
D7.3	Initial Exploitation Report	M12
D7.5	Intermediate Exploitation Report	M30
D7.7	Final Exploitation Report	M42

This deliverable has consolidated a list of exploitable assets being developed (see Section 3) and how they will be made available as a result of the project. It gives an overview of management of knowledge and Intellectual Property Rights (IPR), and the different strategies for how to best utilize all exploitable assets. It also provides an overview of the current exploitation plans of each partner.

2. Management of Knowledge and Intellectual Property Rights (IPR)

The ownership and access to key AMPERE knowledge (IPR, data etc.) is an essential part of the Consortium Agreement (CA) signed by all partners. All IPR provisions follow the spirit of the H2020 programme framework. The Section 3 "Rights and Obligations related To Background and Results" of CA defines the pre-existing partners' know-how and describe the provision of its exploitation, the ownership of the project's results. Ownership of intellectual property shall be shared where there is joint invention. CA defines and regulates in detail the use of:

- **Background knowledge**. Information that can be relevant for the execution of the project, held by the partners prior to project start or acquired outside the project during the same project period. Access rights to this knowledge is available to all partners only if they are valuable or useful for carrying out project activities. Information may include (among others) the set of tools and software components integrated in the AMPERE ecosystem, i.e., model-driven approaches, parallel programming models, existing synthesis tools, compilation, operating systems and hypervisor, timing and schedulability analysis tools, energy models, resilient solutions, run-time parallel frameworks, offloading mechanisms, etc.
- **Foreground knowledge**. Results generated as an activity of the project, independently of whether they can be protected or not. Results may include (among others) new model-driven and parallel programming model extensions incorporating functional and non-functional information included in the meta-models, compiler techniques, multi-dimensional optimisation synthesis methods, timing analysis and scheduling techniques, energy efficiency methods, resilient solutions, functional safety mechanisms, operating systems, run-time libraries, parallel programming models, applications, publications, reports, deliverables, roadmaps, etc. In general, all partners are bound by the terms and conditions of the Commission's contractual rules and a specific piece of foreground knowledge is the property of the partner(s) who has/have generated it. Each partner may use the results and material produced within the project for project purposes provided that such use does not come into conflict with the terms of the project Grant Agreement or the European legislation.
- **Patents**. In case a partner wants to submit a patent application, it must first inform the GA about its intention. The GA is in charge of handling any potential conflict prior to filing a patent. In case a conflict arises, all involved partners will notify the project coordinator that will guarantee that all partners are correctly represented and will guide the negotiation. Any conflicts will be addressed following the conflict resolution process presented in Section 3.2.3. Information of patent applications will be made available to the EU through regular management reports. The costs of the patent will be covered by the submitters.
- **Software/hardware accessories**. The software and hardware accessories from AMPERE partners (e.g. tools, components, devices, programs) required by other AMPERE partners to fulfil the project objectives shall only be used for the purpose of the project. Software products shall be made available free of charge, and hardware products at base costs including handling fees and depreciation. All these items shall be deleted or returned after the end of the project. These agreements shall be extended beyond the duration of project at partners' discretion.
- **Open Access**. The consortium is committed to provide at least green open access wherever feasible following the provisions of Horizon2020 guidelines. Green open-access is also known as self-archiving and means that authors deposit a preprint, a potentially revised author version or, where possible, a final peer-reviewed publisher's version of their publication at an institutional or subject repository that allows public access. Following open access policies of key publishers in

our field (including SPRINGER, Elsevier, JSA, ACM, and IEEE) we have budgeted minor publication costs to allow for limited payments for open access.

3. Exploitable Assets

AMPERE devises a complete system design and computing software ecosystem including the stack for designing, implementing and efficiently executing dependable and physically-entangled systems on platforms composed of the most advanced COTS energy-efficient parallel heterogeneous architectures. With the objective of reducing the time-to-market and thus maximising exploitation opportunities, the AMPERE ecosystem is based on existing technologies owned by AMPERE partners or by external stakeholders, like the openMP parallel paradigm owned by openMP ARB, member of the Ampere IAB (except GNU tools, which are open-source). Moreover, AMPERE develops a powerful interface among the different technologies to facilitate its integration on different development environments (supporting different parallel heterogeneous platforms). This has been identified as a fundamental mechanism of the AMPERE ecosystem for successful exploitation after the end of the project.

Table 2 describes the different software layers and identifies the initial set of technologies that we aim to incorporate into the AMPERE ecosystem, showing the corresponding owner (when known or relevant) and license of each tool. From a bird's eye perspective, SSSA support hardware layer optimization, BOS/BSC/ISEP/TRT optimal software use (e.g. in combination with OpenMP) of hardware resources and ETHZ provides energy optimizations. SYS and EVI provide operating system support and THALIT validates the key exploitable assets in use cases.

The AMPERE consortium has updated and assessed the list of key exploitable assets (KER) using the H2020 approach [EU22]. Individual KERs have been evaluated against the H2020's result maturity level matrix shown in Figure 1 to specify the stage of the project's results and readiness of technologies developed in the scope of AMPERE project.

					4-R&D Technology Demonstration (TRL 5-6)										
			3-R&D Technology Development (TRL 3-5)												
		2-R&D Research for Feasibility (TRL 2-3)							6-Demonstration - System Launch and Operations (TRL 8-9)						
	1-R&D - Basic technology Research (TRL1-2)					5-Demonstration - System Development (TRL 6-8)				7-Market Deployment					
TRL - Technology Readiness Level	1	2	3	4	5	6	7		8	9					
	Basic principles	technology Concept	Experimental Proof of concept	Validated in LAB	Validated in relevant environment	Demonstrated in relevant environment	System Prototype / Demonstration in operational environment		System complete and qualified	System proven in operatrional environment					
CRL - Commercial Readiness Level			1						2		3		4	5	6
			Hypothetical commercial proposition						Commercial Trial		Commercial scale up		Multiple Commercial applications	Market competition driving widespread deployment	"Bankable" grade asset class
IRL - Investment Readiness Level					1		2	3	4		5	6	7	8	9
					First pass canvas		Market Size / Competitive Analysis		Low Fidelity MVP (Minimum-Viable-Product)		Product/market fit	Validate customers, market, revenue streams...	High Fidelity MVP (Minimum-Viable-Product)	Validate key partners, activities, resources, cost structure...	Metrics (revenue, sales, social media influence ...)

Figure 1. H2020's project result maturity level matrix

Table 2. AMPERE System Design and Computing Key Exploitable Assets

AMPERE stakeholder (if different: owner)	Name of asset	License	URL	Relevant AMPERE publications, if any (see Section 8)	Key exploitable assets developed in AMPERE	Identified user communities	Specific actions to address target users and actions, if any	TRL	CRL
BOS	DSML Extensions	Eclipse Public License 2.0	APP4MChttps://gitlab.bsc.es/ampere-sw/wp2/amaltheahttps://www.eclipse.org/app4mc/	[KQTZ21] [MQPHZR22]	Extensions to capture modern pub/sub middleware architectures like AUTOSAR Adaptive, & ROS2) and capture implementation variants of the same functionalities (specialization)	Automotive	N/A	5	N/A
BOS	Dynamic Memory Bandwidth Control	N/A	Proprietary	[SaDZRRPHMGS], [SaHDZMSGM23]	Efficient and dynamic regulation of memory interference	Automotive	N/A	5	1
BOS	APP4MC - Synthetic load Generator (SLG)	Eclipse Public License 2.0	APP4MC		Generation of synthetic code mimicking the performance behaviour of an APP4MC model including middleware communication stubs, e.g. ROS2 (internal and proprietary version for AUTOSAR ADAPTIVE)	Automotive	N/A	5	1
BSC	Extension to APP4MC SLG	Eclipse Public License 2.0	https://gitlab.bsc.es/ampere-sw/wp2/amalthea	[KQTZ21]	Support to parallel and heterogenous execution	Automotive	N/A	5	N/A
BSC	Ampere extensions to OpenMP	Open source	https://www.openmp.org/	[YRQ21]	SW redundant execution mechanism; compatible execution with AMALTHEA; dynamic specialization of functionalities	Automotive; HPC, critical systems	N/A	5	N/A
BSC	Extensions to LLVM	Apache 2.0 with	https://gitlab.bsc.es/	[YuRQ20c] [MRFPQ	Correctness techniques for parallel execution;	HPC, critical systems	N/A	5	N/A

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		LLVM exceptions	ampere-sw/wp2/llvm	]	heterogenous execution support				
BSC	Extensions to KMP	Apache 2.0 with LLVM exceptions	https://gitlab.bsc.es/ampere-sw/wp2/llvm	N/A	Efficient executions	HPC critical systems	N/A	5	N/A
ETHZ	Energy Analysis Tool: Voltmeter:	Open source	https://gitlab.bsc.es/ampere-sw/WP3/voltmeter	[MBFB22]	Analysis and optimization tool: power & performance counters profiling tool, used to collect the dataset to train our power models used for energy optimization (WP3 for offline optimization, but the resulting models are also used in WP4 for online energy monitoring)	Researchers and industry practitioners from embedded systems and HPC communities	Published in open-source on a public repository	3	N/A
ETHZ	Power modeling API	Open source	https://gitlab.bsc.es/ampere-sw/WP3/power-modeling	[MBFB22]	Exposes a user-friendly API to get power/energy estimates at different levels of granularity (CPU, individual core, GPU, etc...) from our power models; it is used for the integration of our work in the multi-criteria optimization flow (WP3)	Researchers and industry practitioners from embedded systems and HPC communities	Published in open-source on a public repository	3	N/A
ETHZ	Online energy monitoring:	Open source	N/A	TBD	Run-time service and API	Researchers and industry practitioners from embedded systems and HPC communities	Publish in open-source on a public repository (TODO) Publish Paper	3	N/A
EVI	ERIKA Enterprise	Proprietary/ AUTOSAR	https://www.erika-enterpr	[CSOWB23]	Operating system Developed in AMPERE: RISC-V porting, Micro-ROS	ERIKA is an AUTOSAR-compliant ASIL-D RTOS. Target	The exploitation role is to	6	2

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			ise.com/		integration	users are AUTOSAR members who design automotive ECUs;	validate the tools via the demonstrator.		
ISEP	Timing Analysis Tool	N/A	Analysis and testing tool	N/A	N/A	OEM, Tier 1, Tier 2, HiPEAC Network Researchers from Academia and Industry, BDVA, SAE Related DIH	N/A	4	N/A
SSSA	Code generator for FPGA accelerated runnables	MIT License	https://gitlab.retis.santannapisa.it/ampere/amalthea-codegen-linux	N/A	Code generator for FPGA accelerated runnables	Researchers and industry practitioners from Embedded Systems, MDE, Real-Time and HPC Communities	Publish in open-source on public repository (DONE) Publish papers (WIP) Showcase its use at some event (TODO) Integrate with APP4MC toolchain (TODO)	5	N/A
SSSA	DART	GPL v3.0	https://github.com/fred-framework/dart	[SPBB21] [CPBD22]	DART hardware synthesis and optimization tool	Researchers and industry practitioners from Embedded Systems, MDE, Real-Time and HPC Communities	Publish in open-source on public repository (DONE) Publish more papers (WIP) Showcase its use at some event (TODO)	5	N/A
SSSA	FRED	GPL v3.0	https://github.com/fr	[SPBB21]	FRED run-time for time-scheduling of hardware Ips on	Researchers and industry practitioners	Publish in open-source	5	N/A

AMPERE stakeholder (if different: owner)	Name of asset	License	URL	Relevant AMPERE publications, if any (see Section 8)	Key exploitable assets developed in AMPERE	Identified user communities	Specific actions to address target users and actions, if any	TRL	CRL
			ed-framework/fred-framework		FPGA slots using DPR	from Embedded Systems, MDE, Real-Time and HPC Communities	on public repository (DONE)		
SSSA	FRED client	LGPL v2.0	https://github.com/fred-framework/fred-linux-client-lib		Linux client for running FRED on Linux	Researchers, automotive industry	Publish in open-source on public repository (DONE)	5	Done
SSSA	meta-fred	MIT License	https://github.com/fred-framework/meta-fred	N/A	Yocto layer for building FRED-compliant Linux image for ZCU102 board	Researchers and industry practitioners from Embedded Systems, MDE, Real-Time and HPC Communities	Publish in open-source on public repository (DONE) Publish more papers (WIP) Showcase its use at HiPEAC	5	N/A
SSSA	Linux Kernel SCHED_DEADLINE variants	GPL v2	https://github.com/thymbahutymba/linux/tree/v5.7-apedf	[SCAO21] [CuAb21]	SCHED_DEADLINE variants (Adaptive Partitioning and Energy-Aware)	Linux community	Publish Papers (DONE) Add energy-awareness (DONE) Perform Evaluation (DONE) Showcase at OSPM2023 (DONE)	5	N/A
SSSA	PARTSim	GPL v2	https://github.com/gabrielebara/PARTSim	[ACM22]	Power-Aware Real-Time Systems Simulator	Researchers and industry practitioners from Embedded Systems, Real-Time and HPC Communities	Publish papers (DONE) Showcase at HiPEAC workshop	5	N.A.

AMPERE stakeholder (if different: owner)	Name of asset	License	URL	Relevant AMPERE publications, if any (see Section 8)	Key exploitable assets developed in AMPERE	Identified user communities	Specific actions to address target users and actions, if any	TRL	CRL
SSSA	PARTProf	GPL v2	https://gitlab.retis.santannapisa.it/parts/partprof	[ACM22]	Power-Aware Exec-Time Profiler	Researchers and industry practitioners from Embedded Systems, Real-Time and HPC Communities	Publish papers (DONE) Showcase at HiPEAC workshop	5	N.A.
SYS	ElinOS	GPLv2	https://www.elinos.com/	N/A	Ported ROS2 library with DDS communication to run on top of ELinOS.	Grow ROS2 and DDS ecosystem. See e.g. https://www.youtube.com/watch?v=Fp0XKJnVoyw	Develop RTI/DDS product.	9	2
SYS	PikeOS	Proprietary	https://www.pikeos.com/	N/A	Ported PikeOS to UltraScale+ and OpenMP library to run on top of top of PikeOS.	Offer OpenMP support. https://www.sysgo.com/blog/article/real-time-operating-system-hypervisor-pikeos-5-supports-openmp	Part of offering	9	2
TRT	Capella bridge with AMALTHEA	Eclipse Public License 2.0	https://github.com/eclipse/capella/blob/master	N/A	N/A	DSML: OEM, Tier1, Tier2	N/A	5	2

4. Exploitation Strategy

Due to the different business interests of the AMPERE project partners, several approaches are used in order to consolidate the results and to raise awareness and their take-up. As for now the project is still in its medium stages and without complete knowledge of what the final results of the project will be, we expect the following approaches to be the most relevant ones for AMPERE.

4.1. Licensing

The AMPERE ecosystem is composed of tools (see Table 2 for the complete list) that either already had existed (open-source and proprietary) or had been developed as needed, e.g. the synthesis tools. Also, in task 5.2 an enhanced version of Linux to be run on the selected platform has been developed. All Linux kernel source code developed within this task have been released through the popular platforms (e.g., GitHub) and the typical communication channels (e.g., Linux Kernel Mailing List and Linux conferences). There are several advantages in adopting an open-source model, including effort and time-to-market reduction by re-using existing code, free help and support from a community of developers and potentially better code. In any case, it is important to understand the obligations and the dynamics of an open-source model, ensuring compliance with specific licenses and, at the same time, allowing effective exploitation activities that will not negatively affect the revenue streams for involved partners.

The AMPERE project has leveraged the long experience of partner EVI, who has successfully adopted an open-source business model for more than a decade. In particular, the AMPERE consortium carefully has selected the best license for each new open-source component developed in the project.

As can be seen in Table 2, components developed in AMPERE use permissive [FOSSA22] open source licenses such as Eclipse Public License 2.0 or Apache 2.0 and restrictive open source licenses such as GPLv2. The use of permissively licensed open source software by restrictively licensed open source software is no problem. The other way around, the shipping of restrictively licensed open source software by permissively licensed software is not generally acceptable. But this not the case in AMPERE.

In particular, to allow easier adoption of the FRED Client library, after discussion within the consortium on the choice of license in autumn 2022, the license was changed from LGPLv3.0 to LGPLv2.0, to address automotive concerns that GPLv3.0's anti-Tivoization clause may limit the right of car producers to lock down components, which in the automotive domain is needed to ensure user safety [Fos15].

4.2. Integration of new software components and tools

Probably, one of the major challenges for an efficient exploitation of the AMPERE ecosystem is its capability to integrate new software components and tools to cope with the requirements that different application domains must face. It is therefore of paramount importance to facilitate the interoperability among the different tools to exploit AMPERE in multiple domains. An interoperability interface has been identified as a fundamental mechanism of the AMPERE ecosystem for exploitation success after the end of the project. AMPERE includes a specific work package (WP6 - AMPERE System Design and Computing Software Ecosystem Integration) to address integration and interoperability issues among tools, and includes two different use cases (with different requirements) to ensure a proper assessment of tool integration features.

In that respect, AMPERE partners BSC and ISEP have developed a powerful interoperability interface, based on the JSON format, capable of gluing the different tools and its interaction to properly cover different development necessities. The interoperability interface had originally been envisioned as a C interface (described in Deliverable 2.2 [D2.2]); it has then evolved to be a JSON data structure that avoids unnecessary elements required by the C language and includes only information relevant for the

integration of the different analysis tools. In a nutshell, the JSON structure contains the task dependency graph (TDG) representing the parallel structure of an OpenMP application, further augmented with information specific to each task, such as the execution time and PAPI (Performance Application Programming Interface) counter measurements (e.g., cache misses, instructions per cycle, etc.). The JSON structure is originally generated by the LLVM compiler (although Deliverable 6.2 [D6.2] indicated Mercurium, all the required techniques have been migrated to LLVM), to later be consumed by the different analysis tools optimizing performance, timing and energy. These tools can introduce modifications in the data structure, which are then merged into the C file containing the TDG that is fed to the runtime system to orchestrate the parallel execution. The tools and documentation required for the generation and use of the interface are publicly available in https://gitlab.bsc.es/ampere-sw/wp2.

Moreover, in the Task 5.4 the hypervisor is enhanced to provide a Hardware Abstraction Layer (HAL) that will facilitate porting the AMPERE ecosystem to different COTS parallel heterogeneous computing platforms. To evaluate this feature, two different parallel platforms [D5.1] have been selected for each use-case [D1.1].

4.3. Standardization

The AMPERE project has provided a roadmap on with recommendations to different standardization committees (D7.8), to increase the synergies and collaboration between industrial and academic communities, and to align AMPERE to engineering practices and tools for current and future CPSoS development, allowing to efficiently uptake of the work after the end of the project.

4.3.1. Safety Standards

Functional safety refers to the property of the system to guarantee its correctness. It is verified by means of safety standards, which impose the code to be developed and analyse in a certain way (ISO26262 [ISO26262], IEC61508 [IEC61508], EN50126 [EN50126], EN50128 [EN50128] and EN50129 [EN50129]). Those standards are of paramount importance to provide trust to system developers and end-users on the correct functionality of the underlying CPSoS controlling the product, in this case a car or a train. Unfortunately, the usage of parallel heterogeneous computing platforms in such systems is still challenging. Safety standards are a barrier to adopt parallel execution in general.

To do so, the task 1.3 evaluated the functional safety aspects required at each integrity level defined in the safety standards ISO26262, IEC61508, EN50126, EN50128 and EN50129, which special interest on the isolation features required by each standard. Based on investigation results from this task, AMPERE has developed a roadmap to provide inputs to automotive and railway safety standards ISO26262 and IEC61508, EN50126, EN50128 and EN50129, to which BOS and THALIT are members of the respective standardisation committee.

4.3.2. Software and System Architecture Standards

Also thanks to the experience about the Data Distribution Service (DDS) gained in the AMPERE project, especially when used on small AUTOSAR RTOSs, the partner EVI started the standardization of DDS in the AUTOSAR Classic standard. In particular, EVI proposed the Concept 707 to the AUTOSAR Consortium, being the official Concept Owner and leveraging the support of the Indian branch of Bosch, who acted as Concept member. The proposed additions to the AUTOSAR Classic specifications have been succesfully integrated in the R22-11 release of the standard (in December 2022) [AUTOSAR-DDS].

In the task 1.4 of the project, the DSML and parallel programming model are extended to better capture functional and non-functional constraints, with the objective of deriving a more efficient parallel transformation. Based on the outcomes of this task we also intend to propose recommendations to the AUTOSAR and OMG UCM standardization committees to better satisfy and secure composable features,

and so enabling more efficient integration of new smarts functionalities into existing dependable and physically-entangled systems without compromising system security.

The AUTOSAR [AUTOSAR] DSML is regulated by an international committee, which provides development guidance and certification considerations to developers, facilitating the integration of components from multiple suppliers, and the verification of the correct functionality of the systems by means of isolation. Similarly, parallel programming specification committees, e.g. the IAB member OpenMP ARB or the OpenCL Khronos group, are in charge of overseeing the parallel programming model specification and produce and approve new versions of it to ensure an effective parallel computation within the new parallel and acceleration computing devices.

4.4. Open Access

The consortium is committed to provide at least green open access wherever feasible following the provisions of EU Horizon 2020 guidelines. Green open-access is also known as self-archiving and means that authors deposit a preprint, a potentially revised author version or, where possible, a final peer-reviewed publisher's version of their publication at an institutional or subject repository that allows public access. As described in the dissemination report, this has been done already for 27 publications and presentations linked from the website (https://ampere-euproject.eu/results/publications). The project results disseminated as open data will also include the used benchmarks and evaluation results. This set of outcomes will provide sufficient evidence to appreciate the viability of the solutions in AMPERE and will enable, in subsequent research, to increase their Technology Readiness Level. Data will be shared with scientific peers to further the build-up of the AMPERE breakthroughs along the concepts of reproducible research.

As described in the dissemination report, wide dissemination is being actively pursued by releasing all technical deliverables in the public domain (https://ampere-euproject.eu/results/deliverables) and by posting the project results as open data in a public open-access repository.

In the task 8.3, the deliverable D8.3 Data Management Plan (DMP) [D8.3] has provided an analysis of the main elements of the data management policy that is being used by the applications with regard to all the datasets that will be generated by the project, has been prepared according to the Guidelines on Data Management in H2020 and delivered at month 6. The deliverable DMP describes the data management life-cycle for all datasets to be collected, processed and/or generated along the lifetime of the project, and is applied to all datasets to be generated by the project.

4.5. Target Users

An important activity of AMPERE towards the dissemination and exploitation of its technology is to establish links to existent communities, targeting tools for system design, to promote, raise awareness and take-up of the project results. As a part of this activity, it is also important to identify early adopters and followers who directly use the technology developed in the scope of AMPERE at the first place. See dissemination report.

5. Current Market Analysis

Global economy and all industries are in turmoil as the coronavirus spreads across the world. As the situation continues to evolve, this section provides up-to-date market analysis.

The global embedded system market includes Tier 1 and 2 manufacturers such as NXP semiconductor, Infineon technologies, Intel corporation and STMicroelectronics which have their manufacturing facilities around the world. The COVID-19 pandemic had affected the operations and, with a reduction of electronic devices demand in 2020-2021, the revenues of such semiconductor based technology providers. At the same time, the decreasing sales in the automotive sectors, consumer devices, aerospace and communication market have negatively impacted the overall semiconductor and embedded system market during COVID time, while the healthcare industry has been greatly growing due to extensive demand of ventilators and other advanced medical equipment across the globe. According to the market research the embedded system market is estimated to be US$ 86.5 billion in 2020 and projected to reach US$ 116.5 billion by 2025 [Icrowd20]. The main factors which are expected to fuel this growth in the coming five years are the current research and development activities in embedded system, rise in the demand of medical devices, smart energy devices, advanced driver-assistance systems (ADAS), portable devices, industrial automation and use of multicore processor and parallel heterogeneous computing platforms. After COVID-19, chip demand in automotive has spiked to the other extreme. However, this overall post COVID recovery has been dampened by economic crisis triggered by the 2022 Russian invasion in Ukraine [PG22, Gr22].

AMPERE is focusing on major embedded domains including but not limited to automotive, railway, industry automation and IoT by developing a software solution and analysis tools for the new heterogenous computing platform. The need of integrating heterogenous application is arising not only in the transport sectors such as automated driving and train control system, but also in other segments like industrial and consumer electronics. AI and machine learning technologies are key to the current revolutionary era of industrial and smart devices. These AI-enabled smart devices require high processing power and real-time system support which can be nowadays provided by parallel and heterogenous computing platforms. In this context, the AMPERE solution will contribute to the overall growth of the embedded system market, especially impacting the European industry in automotive and I4.0.

In the automotive industry the solution for different car domains such as the cluster display, ADAS and ECUs needs to meet constraints related to real-time response, and this meeting of real-time constraints must be eventually demonstrable for certification. The ability to perform the safety function is described in IEC61508 by Safety Integrity, which is a measure of the likelihood that a safety-relevant system will perform the specified safety functions under all specified conditions within a specified period of time. The highest safety integrity level (SIL) is defined by the hardware. The software inherits its SIL and must follow the processes specified in the corresponding software security standard. The IEC61508 has five levels SIL 0 to SIL 4, the ISO 26262 is based on four levels ASIL A to ASIL D (ASIL = Automotive SIL). By separating applications of different criticality, the cost of certification can also be significantly reduced in railway applications, as the entire system no longer needs to be certified at the highest required ASIL level. In addition, certified software components can be offered as COTS components and can be used in various projects without re-certification. For hardware, however, this approach traditionally does not work because it is usually constructed from different components that are currently inseparable, although the ecosystem may become somewhat more flexible due to the gradual adaptation of e.g. chiplet approaches. Nevertheless, the use of a common hardware platform leads to significant savings in procurement, development, and operation.

5.1. Market Situation: Automotive

According to the Statista research department [Stat22a], the worldwide car sales have decreased by over 17% in 2020 due to the coronavirus pandemic, despite the pre-pandemic prevision of a global car sales increase by 6% to reach the goal of 80 million sold cars. Due to the successful containment strategies, measures and government support, the economy in all major sectors is showing signs of recovery which is providing a lifeline for major manufactures in all part of the world. Global car sales have rebounded by 4.5% in 2021 (66.7 million units) and further rebounding in 2023 [Stat23a]. ABI research expects 115 million global car sales by 2025 [ABI20].

The trend towards higher levels of driving automation as well as the centralization of embedded Electrical/Electronic (E/E) architectures has led to a dramatic increase of complexity and required computation power for a lesser number of electronic control units. The resulting vehicle computers are one of the most demanding design endeavors in current cyber-physical systems industry. They are truly cyber-physical systems of systems (CPSoS) in the sense that multiple CPS which have previously been developed independently are now integrated and novel functionalities are developed on top of them in order to realize additional benefits for customers and society. Furthermore, these vehicle computers are developed by a multitude of partners supplying and integrating parts and functionalities on different levels and in several stages.

Thus, the goals of the AMPERE project are very relevant for the automotive industry and the deliverables: in-vehicle software components as well as the tool environment are expected to play a significant role in the developing of vehicle computers. However, the democratization in the adoption of vehicle computers, requires that the underlying modeling and programming concepts will be widely adopted and aligned to international standards. Thus, a close calibration with existing DSMLs (AUTOSAR Classic and Adaptive) as well as a low entry financial barrier and vendor-independence are very important. For this purpose, the AMPERE ecosystem features the AMALTHEA system model, an open source system model adopted by many automotive players, as a central entry point for the automotive domain. Following this strategy, extensions and basic tooling have been made available as part of the Eclipse project APP4MC, which is the development environment around AMALTHEA.

5.2. Market Situation: Light Railway

Covid-19 also hit the railway industry globally. The revenue has decreased by 37.1% in 2020 according to Statista research department, but again it is rebounding [Stat23b]. However, fortunately due to remarkable advancements in the preparation of vaccine and containment measures the industry is showing signs of recovery. The annual growth rate is predicted to increase by 16.8% (CAGR 2020-2025) to reach the projected market volume of US$149,387m by 2025 [Stat22c]. Annual market size of the rail control for Light Rail Systems is 1.1 Bn € and it is expected to grow 1.9% per annum in the future years.

The Light Rail Transit or tram market lacks global standardization and the segments are divided by geographic area and mode of use. Europe and APAC are using similar approach compared with Middle East or NAFTA area. Tram, LRT, Tram-Train or Tram-Metro may differ according to requested performance and physical constraints.

A major trend to “Autonomous Vehicle” also influences the railway world. However, public transport systems still rely on legacy technologies invented in the past century to ensure the safe movement of their users, especially in Signalling systems. The window of this market creates opportunities to innovative companies to introduce more smart systems to the industry. Europe is the area with more than 35000 Light Rail Vehicles in operation. Thus, for technology transformation in this sector the Europe would be the reference market as a showcase for a wider world market.

Self-localization and obstacle detection are an important and challenging issue in current driving assistance and autonomous driving research activities. Innovative methods for localization, awareness of surrounding environment and mapping will impact, in the next years, the railway world to introduce new technologies available today to Railway Signalling with application of them within the Safety Domain.

6. Individual Exploitation Plans

This section contains the individual partner exploitation plans describing the activities done and planned to promote use of the technologies developed during and after the project end.

6.1. Final Exploitation Plans From Academic Partners

The exploitation plan and interests described by research partners are the following:

- To extend the capabilities of the system modelling and specification language technologies with additional features for parallel programming model and heterogeneous platforms;
- To research for various system models (AUTOSAR, CAPELLA, AMALTHEA) for new reference system design and computing software ecosystem for future dependable and physically entangled systems with high-performance requirements.
- To investigate further techniques and methods for the integration of parallel programming models and real-time analysis techniques, targeting more accurate and realistic analysis methods;
- To investigate reliable, robust and energy-aware solutions for autonomous and safety-critical systems;
- To evaluate engineering techniques supporting the design operation continuum of dynamic CPSoS and emerging technologies such as big data analytics or artificial intelligence.

The AMPERE project results aim to lead to new research lines to in order to contribute to the continued evolution of the AMPERE model-driven framework.

6.1.1. Exploitation Plan of Partner (SSSA)

SSSA exploitation plans for the project concern mainly 4 areas:

- Hardware and software developers' communities
- Linux kernel community
- Academic real-time research community
- Automotive model-based community

Concerning hardware/software developers' communities, SSSA has released the FRED framework for Ultrascale+ and a few other Xilinx boards on Linux as open source, together with its accessory hardware designs and demos. The released software is available through the general website at http://fred.santannapisa.it/, where the latest version of the software can be downloaded from https://github.com/fred-framework, where a set of repositories and open-source tools are available for download, compile and use. Among these, fred-linux is the general FRED framework that can be compiled on a Linux OS running on bare-metal on a range of DPR-capable Xilinx boards. Additionally, fred-elinos is a ready-to-use package made available to use the technology on the Ultrascale+ SoC board, under the PikeOS hypervisor. The fred-docs repository includes all the documentation a user needs to get started with the FRED framework, including the use of the open-source DART tool for compiling new hardware designs to be deployed as accelerators with FRED. Xilinx has also been informed about the realized FPGA-related tools, in order to push for a wider adoption and magnify the impact of AMPERE in the development of next-generation CPSs that require FPGA-based hardware acceleration.

For what regards the Linux kernel community, exploitation plans of SSSA are to trigger fruitful discussions about the progress made within AMPERE on the side of energy-aware scheduling of real-time tasks on heterogeneous platforms. In this area, SSSA is integrating the mechanisms investigated in AMPERE within the SCHED_DEADLINE code base [LSAF16], which is a mechanism originally developed jointly by SSSA and EVI, and still actively contributed to by both partners, and release any code as open-source patches.

Therefore, SSSA can operate alongside three main channels. First, it can submit possible patches to the SCHED_DEADLINE in-kernel scheduler on the Linux Kernel Mailing List (LKML) for review by the kernel community. Second, it can discuss the patch live at related events organized periodically. AMPERE project partners SSSA and EVI are both involved in the yearly organization of OSPM, the international workshop on energy efficient scheduling in the Linux kernel, which has been organized yearly 2017-2022, with a strong industrial focus. Indeed, the workshop has been organized in close cooperation with, and attended by, major international industrial players and stakeholders in the area, including Intel, ARM, Google, VMWare, IBM and RedHat. The workshop has been organized 3 times in Pisa, the 4th edition was remotely held due to Covid, and the latest edition in 2023 has been organized in Ancona. OSPM constitutes an excellent opportunity to gather feedback from the community of Linux kernel developers actively involved in the continuous improvement of the kernel features, especially on the side of real-time performance of applications. Indeed, during OSPM 2023, SSSA has contributed with two presentations related to the research made in AMPERE:

- Results from using SCHED_DEADLINE for energy-aware optimization of RT DAGs on heterogeneous hardware, by T. Cucinotta
- SCHED_DEADLINE meets DVFS: issues and a possible solution, by G. Ara.

These presentations have been made in front of the majority of key software developers dealing with the development and maintenance of the code-base for the process scheduler and the power management subsystem, in the Linux kernel.

Third, SSSA plans to investigate possible interest by users of the novel real-time mechanisms within the Linux kernel, leveraging the yearly Linux Plumbers Conference (LPC). This is a yearly meeting where many industrial practitioners gather, who are working on Linux from a 360-degrees perspective. This involves kernel main core developers, people working on device-driver development, application and middleware developers, and Linux distributors and maintainers.

SSSA is finally planning to raise the awareness on the predictability of FPGA acceleration and the capabilities of the AMPERE ecosystem in the embedded/CPS and real-time research communities. To this purpose, SSSA, alongside other AMPERE partners, will be presenting their work on the AMPERE ecosystem, in an on-line webinar within the HiPEAC sponsorship, targeting a wide community of researchers and developers working on HPC and embedded and real-time systems. Also, some of the techniques investigated in AMPERE for energy-aware scheduling of real-time workloads, has been prototyped by modifying RTSim, an open-source simulation platform well-known among researchers in the community to simulate the timing of real-time applications, obtaining PARTSim, the Power-Aware Real-Time Systems Simulator. SSSA has also made the final scheduling algorithms for heterogeneous platforms available as an open-source tool that can easily be reused to improve the techniques and develop further research in the area. These are available from the papers published on the topics [SCAO21, CAPDN23].

Additionally, SSSA has been interacting with ETHZ with a PhD student exchange, in order to integrate its own energy-aware SCHED_DEADLINE variant with the energy models realized at ETHZ. This will allow SSSA to realize schedulers for the Linux kernel that are more complete, integrating the on-line energy estimation models from ETHZ.

For what regards the automotive model-based community, SSSA is interacting with Bosch, among others, to implement the modifications needed on the Amalthea models in order to support energy-efficient scheduling of real-time workloads on heterogeneous platforms. At the same time SSSA is taking care of the development of the accompanying analysis, verification and optimization mechanisms, that have been developed as an independent open-source tools to be integrated within the App4MC design workflow. These are available for example from the companion page at https://retis.santannapisa.it/~tommaso/papers/acmtecs23.php, of a paper published on the topic [CAPDN23].

6.1.2. Exploitation Plan of Partner (BSC)

The objective of the Barcelona Supercomputing Center (BSC) is to create a new reference system design and computing software ecosystem upon which the future dependable and physically entangled systems with high-performance requirements will be developed. To do so, BSC has integrated its large experience on parallel programming models (specifically openMP) and the outcomes of the H2020 projects, AXIOM and LEGaTO (addressing energy and fault tolerance with OmpSs@FPGA), CLASS and ELASTIC (addressing real-time big-data analytics with COMPSs), and HP4S (addressing the use of OpenMP is payload systems for the space domain) industrial projects. In that respect, it is worth mentioning that BSC has already successfully developed two reference ecosystems widely used in the HPC, big-data and AI computing domains, i.e. OmpSs and COMPSs respectively. Moreover, the advances of OmpSs has deeply influenced the OpenMP standard.

Finally, BSC will continue the research towards a complete integration of HPC and CPS by targeting further synthesis tools and extensions on well-known parallel programming models to better express functional and non-functional constraints of future dependable and physically entangled systems. This will further enable the adoption of the AMPERE technology to wider application domains, such as big data and AI applications, in which BSC is also very active. BSC has planned synergies with RisingStarts project and to apply the results of AMPERE to precision agriculture projects.

Concerning standardization activities, there are ongoing discussion with standardization body as openMP ARB in order to promote the use of openMP to implement parallelism with safety languages such Ada. All the results from BSC are open source licensed with no permission conflict detected up to this moment among the different technologies developed.

6.1.3. Exploitation Plan of Partner (ETHZ)

ETH Zurich will continue research activities around energy-efficient heterogeneous many-cores, and the integration of such resource-management policies within well-established parallel programming models for such platforms. The increased knowledge in this area will:

- foster the education and training of experts in the technologies developed in the project, at all levels;
- position ETHZ as a strong industry-oriented applicative research partner.

Towards the end of the project, the developed technologies will reach the adequate maturity for industrial uptake. These technologies will be evaluated in cooperation industrial partners (including discussions with IAB industrial partners) strengthening ETHZ as a key partner for future technology transfer initiatives. Furthermore, the commitment of AMPERE to interact with the European Processor Initiative (EPI) project and the use of HERO as a proto-typing platform, enables reinforce the ETHZ as part of the RISC-V foundation as a leader in in promoting the adoption of RISC-V based technologies.

The maturity of power and energy management software and hardware layers developed within AMPERE will also enable ETHZ to push these techniques to broad audiences through its open-source PULP and HERO platforms, to maximize their impact in both industry and academia.

6.1.4. Exploitation Plan of Partner (ISEP)

ISEP will exploit project results through further research and development activities on the integration of parallel models and real-time analysis techniques, targeting more accurate and realistic analysis methods and fostering the use of the combined techniques in real-time embedded applications. In particular, ISEP will continue the work on the integration of the real-time parallel technology created in AMPERE to be

used in critical systems, using OpenMP, Ada and Rust technologies, also targeting the usage of RISC-V processors, in the scope of follow-up collaborations and projects.

ISEP will exploit these results with the companies in AMPERE, and in its IAB, addressing the transfer and take-up of results in the industrial domain, in cyber-physical systems in general, but with particular focus in rail and automotive. The outputs of ISEP in the project will be also integrated in the AMPERE framework, and exploited together with the project partners.

The knowledge obtained in the project will also be explored through publication of scientific results in international events and journals, and integration in the master and doctoral programs, where the ISEP team is involved, such as the existing master on critical computing systems engineering, and the forthcoming doctoral program in engineering of intelligent systems at ISEP.

6.2. Final Exploitation Plans From Industrial Partners

The exploitation plan and interests that are typically described by industrial partners are the following:

- To productise the technologies developed within the AMPERE project to make them available as software tools and platform offers for the industry domains targeted by each partner;
- To use AMPERE technologies for development of dependable and physically-entangled systems in their respective industrial domains;
- To encourage their suppliers to utilise AMPERE technologies for the development of parallel critical real-time smart systems;
- To establish distribution of AMPERE technologies in markets addressed by each partner;
- To conduct promotional and marketing actions to create further awareness of the new AMPERE tools for addressing heterogeneous platforms and parallelised software development;
- To undertake further development of AMPERE technologies as enhancements and updates to provide improvements and greater stability in the prototype technologies from the project;
- To expand the portfolio of related products by collaborating with other organisations that can provide additional tools and platform technologies;
- To leverage the expertise and know-how gained in the AMPERE project to make innovation, designing novel technology or entering different markets;
- To support the take-up of AMPERE project technologies through awareness building amongst the European software development community.

In carrying out the above exploitation actions, all industrial partners will seek to create revenues and other commercial opportunities as important actors within the AMPERE project.

6.2.1. Exploitation Plan of Partner (EVI)

The work done by EVI in AMPERE allowed the company to enhance its AUTOSAR Classic solution based on the ERIKA Enterprise RTOS, being able of creating a competitive product for the European automotive market. The main exploitable results hasconsisted on the support for both SYSGO's PikeOS hypervisor and RISC-V technology (expected to become more and more strategic in the forthcoming years). The exploitation plan for these parts will need to take into account potential licensing constraints imposed by the AUTOSAR consortium. The exploitation activity will then naturally flow through Evidence's shareholder Huawei, which could complement Evidence's offering with additional hardware and software components add-ons. The marketing activities will mostly consist on meetings with European automotive OEMs and Tier-1s. However, EVI is also collaborating with the other AMPERE partners to organize dissemination events (e.g. participation to conferences and exhibitions, organization of workshops, submission of papers, etc.).

ERIKA Enterprise was originally distributed in dual licensing. The project continued in its closed source form, due to the restrictions imposed by the AUTOSAR Exploitation licensing. After an agreement with AUTOSAR, however, the source code originally available on GitHub has been contributed to the AUTOSAR Consortium under the name of "OpenERIKA", where the "open" means "open for AUTOSAR Members" (note that membership is free for Universities and research institutions). This is a big change for the AUTOSAR Consortium, because in the past only the AUTOSAR Adaptive part of the standard was including free code. Partner EVI is therefore attempting to break a big wall, changing the mindset of the AUTOSAR Consortium to increase quality and competitiveness by becoming more open. In the future, such attempt might lead to the creation of the so-called "Classic Platform Demonstrator" (CPD) which could be composed of OpenERIKA, ARTOP tool and COMASSO BSW (originally based on Bosch codebase). This would enlarge visibility and business opportunities for EVI at the European level. On the other end, it would impact the whole European automotive industry creating a free demonstrator which could be used for educational or even commercial purposes.

In the meantime, the experience gained by EVI during the AMPERE project (specifically, about the DDS protocol) has allowed the company to strengthen its position in the AUTOSAR Consortium, leading some standardization activities and thus increasing networking and synergies with other automotive companies (e.g. Bosch, RTI) which could eventually result in concrete "win-win" business opportunities.

Finally, EVI has also investigated the development of a novel POSIX PSE53 RTOS targeting the automotive market. Such preliminary design is expected to grow through further private investments, becoming a potential AUTOSAR Adaptive solution. Once finished, a proper exploitation plan will be developed, which could consist either on a traditional royalty-based commercial offering or on an open-source business model. To this aim, a survey of both commercial and open-source solutions available has been carried out to identify the best exploitation and dissemination strategies.

6.2.2. Exploitation Plan of Partner (SYS)

SYSGO exploitation plan as stated in the project proposal is to aim to strengthen position of PikeOS on European market which is currently dominated by US companies and create new markets for PikeOS. The strategy to achieve these goals is to constantly innovate in the product line. AMPERE will enable extending the PikeOS functionality to support parallel heterogeneous hardware. The targeted simplicity of programming of heterogeneous hardware will enhance the existing PikeOS market offering for dependability and real-time with cross-layer programming support to reduce programming and integration efforts and shift decision in favour of PikeOS. Existing customers plan and/or have to use highly heterogeneous hardware in next generation systems. Therefore, SYS sees support for parallel heterogeneous platforms as an important milestone. This support shall be easy to use and not introduce technical obstacles.

The exploitation plan is split into two phases during the project and after the project. During the project SYSGO has:

- created awareness of the problem and developed solutions by writing white papers and industry-oriented publications;
- kept main interested partners and customers updated on project intermediate results; e.g. as done here -> https://www.sysgo.com/blog/article/tackling-mixed-criticality-for-automotive
- show-cased project result on the industrial trade shows focused on cyber-physical systems such as Embedded World, RTS, Avionics Europe, SAE, it-SA; -> e.g. work based on ROS see https://www.youtube.com/watch?v=cp6vpyBLGo4
- closely interacted with the product development team to decrease transition into product phase;

- collaborated with RTI on DDS support https://www.sysgo.com/fileadmin/user_upload/data/partner_solutions/SYSGO_Partner_Solution_RTI.pdf
- investigated the exploitation opportunities with the use-case providers.

After the project, SYSGO plans to further extend business on ROS, DDS, which is increasingly adopted in both automotive and railway domains.

6.2.3. Exploitation Plan of Partner (TRT)

One of the TRT's roles in the Thales group is to identify promising technologies and help Thales business units adopt them in order to improve the Thales industrial processes. Because it is a research center within the Thales group, TRT itself has no business plan on its own.

In project AMPERE, TRT brings its expertise in system modelling with its own open-source modeller called CAPELLA implementing the Arcadia methodology to design system architectures. Compared with the other technologies involved in AMPERE, CAPELLA is at a higher level of abstraction. A large part of the partners is working on lower-level models (e.g., code generation for parallel computation, power consumption analysis, timing analysis, etc.) in the scope of AMPERE; TRT aims at gaining expertise in the performance analysis of architectures for high-performance computing, understanding how to address trade-offs between computation time and power consumption for HPC.

The intent of TRT is to gain knowledge in this field and apply this knowledge to Capella to enable the design of system architecture models that contain the necessary information to produce lower-level models for parallel computing architecture. Thus, TRT can assist Thales business unit in designing system architectures that target parallel computing using model-driven engineering (MDE). The MDE community in Thales gathers more than 500 engineers, across all Thales business units; a large part of them works with Capella.

In Ampere, TRT has directly assisted THALIT to validate the feasibility of the Capella modelling approach. Beyond Ampere, TRT will be able to assist other Thales business units – first in the transportation domain, then in the whole Thales MDE community – to help them adopt the Ampere technologies in their design processes.

6.2.4. Exploitation Plan of Partner (THALIT)

Thales Italy (THALIT) has interest in testing and commercially exploiting the AMPERE technology for urban transport applications such as Light Rail Transit (LRT) and urban rail. By leveraging on the technological solutions developed in AMPERE, THALIT strives to improve the innovative autonomous tram solutions and building blocks delivered for the smart urban transport systems.
The Florence tramway receives 14 million passengers each year on its trams (Data 2017). The reasons that lead to the choice of the tramway are comfort, safety, economic convenience and certainty of travel times. The 87% of passengers are overall satisfied with the service and consider it good and excellent.
Due to geographical, infrastructural and socio-economic factors, the city of Florence plays a central role in the mobility scenario of the area, with about 80.000 and 70.000 cars moving respectively to and from Florence every day, accounting for severe traffic congestions and affecting quality of life.

To face these issues, the local governments (municipal, metropolitan and regional) have started a thorough transformation of the public transportation network, which includes the construction of new light rail lines, a complete redesign of the bus service and a widespread use of ICT solutions.

The development of the ODAS for the railway use case in the AMPERE project will contribute in:

1. Decrease the number of accidents in the tramway environment, warning the driver of a potential Acollision with detected target and reducing its reaction time;
2. Improve the state of the art, developing innovative technologies supporting compute-intensive applications in the railway and automotive domains;
3. Develop a meta model-driven abstraction, incorporating functional and non-functional constraints;
4. Reducing the development and integration costs of the ODAS functional critical software modules;
5. Improve object detection capability and reducing false alarms in critical environmental conditions (e.g. rain, fog presence, etc.);
6. Assess the impact of synthesis methods and parallel heterogeneous execution with regard to the safety and security requirements;
7. Extend parallel programming models to make a more efficient use of resilience redundancy techniques.

The key component of the AMPERE ecosystem to fully exploit the performance capabilities of platforms composed of parallel heterogeneous architectures will be the code synthesis tool, interfacing between the Capella DSML and the parallel programming model supported by the platform. The AMPERE project will allow THALIT to create competitive solutions (specifically for the Florence municipality) and make business out of it.

6.2.5. Exploitation Plan of Partner (BOS)

Regarding the prospects of economic success, no changes to the exploitation plan stated in the project description are necessary. However, it is expected that the use of the AMPERE ecosystem will cover a larger circle of users than originally thought. The possibilities of such a system are increasingly attracting interest inside Bosch. More precisely, in several discussions with large ongoing development projects within Bosch, the AMPERE technology gained a lot of interest despite being hindered by COVID-19 restrictions that limited working time.

The reason for that interest is that AMPERE directly addresses the challenges in model-centric development arising from the technology shift from dedicated µC-based to massively parallel and heterogeneous computing platforms. Especially the mapping methodology constructively guaranteeing timing properties has potential to master system complexity, and thus reduce development and validation efforts.

Bosch, therefore, intends, like stated in the project description, to introduce AMPERE methods within 2-3 years after project end into its internal development processes for systems with stringent timing requirements. Additionally, Bosch will actively and continuously participate in the standardization of the key results into industrial standards, especially AUTOSAR and ISO26262, and in already existing development environments such as AMALTHEA, included in the APP4MC Eclipse framework. First activities are already well advanced. For instance, Bosch extended the internal “Synthetic Load Generator” tool to support ROS2 middleware concepts (which are conceptually strongly related to AUTOSAR Adaptive) and made it available via open source for collaboration with partners (internal and external to the AMPERE project). Also, the open source APP4MC Eclipse framework (which is the basis for Bosch internal development across different business units) is currently extended to cope with AMPERE technology concerning the modelling of parallel execution on heterogeneous Systems-on-Chip. This “upstream first” strategy pursued by Bosch within AMPERE is crucial to strengthen the engineering backbone serving as basis for distributed development projects with many suppliers that are common in the automotive domain. This way the AMPERE technology will be broadly disseminated and exploited to its full potential in the automotive industry. On top of that Bosch also patented a novel dynamic memory bandwidth control mechanism [PrNFA], that supports the ISO26262 freedom-from-interference

requirement. Moreover, the scientific potential and success of AMPERE are excellent. Conferences and other events where we contribute and publish AMPERE results are raising the profile of AMPERE, and are creating a wider circle of interest.

6.3. Recommendations to safety standards and joint exploitation

The lessons learned of the project with regards to safety standards are captured in the D7.8 “Roadmap of further research on the implications of parallel execution on the highest safety-critical systems”.

Open source assets (e.g. from academic partners) are made available to industry via publishing at open-source repositories such as Github (see Section 3). Exploitation lines with strong industry support are:

- the APP4MC community from the Eclipse foundation, where BOSCH and THALIT (via Thales) are both members
- the AUTOSAR community for the ERIKA results, where BOSCH is member

Additionally, we have presented joint results at the 24 June 2023 HiPEAC workshop.

Joint exploitation is also realized in the RESPECT project, coordinated by the Barcelona Supercomputing Center and comprised of business mentors BOSCH and AirBus, using the AMPERE- produced Task Dependency Graph for multi-criteria analysis. It expands on AMPERE's results to rise to technology readiness level 6 by consolidating the taskgraph framework, extending and testing features for resilience and consolidating and extending application domains (automotive and space). [Amp23]

Moreover, BOS and SYS plan to use AMPERE results to investigate orchestration in real-time cloud/edge architectures in the context of IPCEI-CIS (Next generation cloud infrastructure and services).

7. Acronyms and Abbreviations

- AI – Artificial Intelligence
- AMPERE – A Model-driven development framework for highly Parallel and EneRgy-Efficient computation supporting multi-criteria optimization
- API – Application Program Interface
- AUTOSAR – Automotive Open System Architecture
- CA – Consortium Agreement
- COTS – Commercial Off-The-Shelf
- CPS – Cyber Physical System
- CPSoS – Cyber Physical System of Systems
- CPU – Central Processing Unit
- DDS – Data Distribution Service
- DMP – Data Management Plan
- DPR – Dynamic Partial Reconfiguration
- DSML – Domain-Specific Modeling Language
- EPI – European Processor Initiative
- FPGA – Field Programmable Gate Array
- GPU – Graphics Processing Unit
- HAL – Hardware Abstraction Layer
- HERO – Heterogenous Research Platform
- IPR – Intellectual Property Rights
- KER – Key Exploitable Result
- MDE – Model-Driven Engineering
- MPSoC– Multiprocessor SoC
- OEM – Original Equipment Manufacturer
- OS – Operating System
- PULP – Parallel Ultra-Low Power
- RTOS – Real-Time Operating System
- SoC – System-on-Chip

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