Ref. Ares(2020)5375803 - 09/10/2020

A Model-driven development framework for highly Parallel and EneRgy-Efficient computation supporting multi-criteria optimisation

D8.4 Progress report for technical review

Version 1.0

Documentation Information

Contract Number	871669
Project Website	www.ampere-euproject.eu
Contratual Deadline	30.09.2020
Dissemination Level	Public
Nature	Report
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Contributors	All partners
Reviewer	THALIT
Keywords	Model Driven Engineering, Parallel Programming Models, Functional and non-Functional Requirements

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 871669.

Change Log

Version	Description Change
V0.1	Initial version by Eduardo Quiñones (BSC)
V0.2	Contribution to WP2 by Sara Royuela (BSC)
V0.3	Contribution to WP5 by Claudio Scordino (EVI)
V0.4	Contribution to WP6 by Sara Royuela (BSC)
V0.5	Contribution to WP5 by SYS (EVI)
V0.6	Contribution to WP3 by ISEP, ETHZ and SSSA
V0.7	Contribution to WP1 by THALIT
V0.8	Contribution to WP7, WP8, sections 7 and 8 by BSC
V0.9	THALIT revision
V0.10	Contribution to WP1 and WP2 by Delphine Longuet (TRT)
V1.0	Version ready to be submitted to the EC

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1. Executive Summary

This deliverable provides the progress report describing the AMPERE project activities performed during the first nine months of the project, from 01 Jan 2020 to 30 Sep 2020 (M1-M9).

AMPERE has been impacted by the Covid19 outbreak, delaying the end of MS1 from 30 June 2020 to 30 Sep 2020. This impact has been heterogeneous on the different WPs: In case of WP2, WP4, WP5 and WP6, tasks (and the corresponding deliverables) have been delayed only one month; in case of WP1 and WP3, they have been delayed three months. These delays are reported in detailed in Section 3.

2. Objectives

This section lists the AMPERE objectives (in *italics* as presented in section 1.1 of the DoA) and describes the work carried out during the reporting period towards the achievement of each listed objective.

The corresponding *Key Performance Indicator* (KPI) associated to each AMPERE objective is not discussed in deliverable yet, due to the requirements gathering nature of the first phase of the project. KPI will be addressed in the following periodic reports, when the developments of the AMPERE use-cases and the SW architecture will be more advanced.

O1. Facilitate the design, development and maintenance of CPSoS implemented with DSML and targeting platforms composed of energy-efficient parallel and heterogeneous architectures

This objective is being addressed by including within the same framework, i.e., the AMPERE SW architecture, all the features needed for the development and efficient execution of Cyber Physical System of Systems (CPSoS) on advanced energy-efficient parallel and heterogeneous architectures. This includes:

- A set of Domain Specific Modelling Languages (DSMLs) upon which the AMPERE use-cases are being developed; concretely AMALTHEA, CAPELLA and AUTOSAR Adaptive. Moreover, a *meta model driven abstraction interface* based on the DSMLs will be used to communicate with the components described below.
- Code synthesis tools and compiler techniques responsible of generating parallel code optimized to fulfill the non-functional requirements (NFR) specified in the DSML and the information gathered by the multi-criterion analysis tools. To do so, a *meta parallel programming model interface* is being developed to facilitate the transformation of the DSML to the *high-level parallel programming models (PPMs)* supported by the underlying processor architecture.
- A set of multi-criterion tools responsible of analyzing and monitoring the NFR of the system. This information will be used by both, the DSML transformation and run-time execute, to guarantee the fulfillment of NFR.
- A set of runtime techniques for the orchestration of the parallel execution and FPGA management, responsible of fulfilling the requirements provided by the multi-criterion analysis and optimization monitoring tools.
- An operating system (OS) and hypervisor component responsable of providing safety and security system guarantees through isolation mechanisms. The hypervisor provides the *Hardware Abstraction Layer (HAL) interface* in charge of interacting with the underlying parallel processor architectures; in AMPERE, the Xilinx Zynq ZCU102 and the NVIDIA Jetson AGX.

O2. Develop (off-line) code synthesis methods and tools for DSMLs capable of: (1) identifying potential parallel software entities and derive an automated and efficient parallel source code supported by the underlying targeted platform; and (2) perform a multi-criteria optimization model transformation, such that the performance is significantly increased, whilst satisfying energy-efficiency, safety and cyber-security, real-time response, resiliency and fault-tolerance, and testability

This objective is addressed by including into the AMPERE SW architecture, the set of tools needed for a productive development of the CPSoS based on DSMLs currently used by the automotive and railway industry. To do so, AMPERE is researching on suitable representations of the parallel behaviour of CPSoS components, based on a *Direct Acyclic Graph* (DAG) or *Task-Dependency Graph* (TDG). The DAG, extracted from the DSMLs, identifies the different parallel entities, communication and synchronization methods, as well as the NFRs associated to each entity and extracted with the multi-criterion tools. This DAG will then be transformed to the PPM supported by the underlying processor architecture. This transformation will leverage the NFR information included in the DAG to guarantee the NFRs, whilst exploiting the parallel opportunities exposed within the DAG and the processor architecture to maximise performance.

The following tools are currently under investigation/development, to be integrated into the AMPERE SW architecture:

1. Automatic code generators integrated in AMALTHEA SW frameworks.
2. Compiler analysis tools based on Mercurium and LLVM.
3. Analysis tools, including support to OpenMP, CUDA and FPGA dynamic reconfiguration,e.g., Fred.

O3. Develop (on-line) run-time techniques capable of: (1) monitoring the parallel execution to ensure that functional and non-functional constraints are guaranteed; and (2) dynamically optimising and distribute the parallel heterogeneous computation to better adapt the execution to new working conditions while respecting the multi-criteria optimization done at development phase

This objective is addressed by including into the AMPERE SW architecture, the set of tools needed for an efficient execution of the CPSoS. To do so, AMPERE is researching on monitoring techniques that, based on the representation of the parallel execution described as a DAG, identify when an NFR is violated, e.g., a deadline is missed. The DAG allows to identify the portion of parallel code that is being executed, and so analyse the impact that this execution has on the end-to-end response time of the CPSoS and apply countermeasures to avoid it.

The following tools are currently under investigation/development, to be integrated into the AMPERE SW architecture:

1. Monitoring mechanisms based on the performance counters available on the selected processor architectures, to capture the metrics needed to identify NFR violations.
2. Run-time frameworks supporting the execution of OpenMP and CUDA PPMs, e.g., GOMP, and FPGA execution, e.g., Fred.
3. Erika OS, ROS2 and PikeOS.

O4. Provide an integrated system design and computing software ecosystem composed of currently existing tools (when possible), capable of efficiently exploiting the performance opportunities of advanced commercial off-the-shelf parallel platforms (supporting many-core fabrics, GPUs and FPGAs)

AMPERE aims to provide a framework ecosystem capable of instantiating different SW architectures configurations, incorporating different software components, with the objective of covering different system requirements. To do so, each software component includes a clear interface to ensure a seamless integration with the rest of components. Moreover, the development of the AMPERE SW architecture involves partners from different institutions and areas of expertise. In order to facilitate the development and integration activities, AMPERE has defined a set of processes and tools.

O5. Use the AMPERE ecosystem to facilitate the development and execution of two real world applications from automotive and railway domains, significantly increasing its performance and fulfilling functional and non-functional constraints

The AMPERE project is considering an Obstacle Detection and Avoidance System (ODAS) from the Light Rail Transit (LRT) domain, and an intelligent Predictive Cruise Control (PCC) system, from the automotive

domain. The two use-case are being developed with the DSMLs provided by the AMPERE SW architecture, with the objective of applying the novel development and execution capabilities aimed by the AMPERE project.

O6. Prove short- and long-term industrial impact and exploitation capabilities of AMPERE

This objective has not been addressed by AMPERE yet. The strategy that the project aims to follow is to address automotive and industrial standards when developing the AMPERE use-cases, concretely the ISO26262, IEC61508 and EN 5012X standards. Moreover, the project will benefit from the know-how of THALIT and BOS partners to apply the same industrial procedures in the development of use-cases, to better adapt the design of AMPERE SW architecture to industrial environments.

Finally, the software components that form the AMPERE SW architecture are either owned by the AMPERE partners or offered as open source with a large community behind, with the objective of reducing the time-to-market and maximize the exploitation opportunities of the AMPERE ecosystem.

3. Explanation of the work carried per Work Package

3.1. WP1 - System Model Description and Use cases

The main objective of WP1, led by THALIT, is to develop and experiment a set of use cases with high-performance and low-energy requirements (among others) implemented with DSMLs, upon which AMPERE will be evaluated. We include:

i. Two real-world use cases from the automotive and railway domains.
ii. A test bench suite composed of small kernels extracted from the real-world use cases, with the objective of easing the interaction among partners and enabling a much earlier evaluation of the work.

To reach this goal, WP1 will:

1. Identify the set of functional and non-functional requirements of each use case and will evaluate whether this information is already included in the corresponding DSML.
2. Develop a new meta-model-driven abstraction capable of expressing:
    i. the key functional and NFR required for an efficient model transformation for parallel heterogeneous architectures, preserving application's semantics;
    ii. computation over tensor data to speed-up AI operations.
3. Extend DSMLs to map with the new features included in the meta-abstraction, allowing a formal analysis of functional and non-functional constraints; and an efficient parallel transformation.
4. Provide recommendations to language standardization committees.
5. Investigate parallel heterogeneous platform vulnerabilities, identifying bottlenecks with respect to functional and timing isolation to ensure composability and cyber-security, and to provide recommendation guidelines to automotive and railway standards to support parallel heterogeneous computing.
6. Analyze safety- aware and security-aware execution models based on platform vulnerabilities analysis and safety and security specifications, to enhance time and space scheduling approaches (within WP4).

Table 1 and Table 2 present an overview of the status of WP1 tasks and the deliverables submitted during the reporting period, respectively.

Table 1. WP1 tasks status overview.

Task	Title	Start Month	End Month	Status
T1.1	System model requirement specification and use case definition	M1	M9 (delayed)	Ongoing
T1.2	Generation of AMPERE test bench suite and use case preparation	M7	M27	Started
T1.3	Functional safety and security	M7	M27	Started
T1.4	Meta model-driven abstraction and model-driven extensions	M7	M27	Started
T1.5	Use case evaluation	M28	M36	Not started

Scheduling of activities was heavily impacted by COVID-19. Concretely, THALIT works were heavily slowed down (almost stopped in the period spanning form M3-M7) and the most evident consequence for T1.1 was the delayed release of D1.1, moved from end of June 2020 to September 15th. Activities relating to other tasks could be started but their initial development is slower than expected without COVID-19. Nevertheless, unless there is a strong resurgence of the pandemic, current delay will be recovered in the next months.

Table 2. WP1 deliverables submitted during the reporting period.

Delive rable	Title	Lead Benef.	Task	Due month
D1.1	System models requirements and use case selection	THALIT	T1.1	M9 (delayed)

Description of progress by partners' contributions during the reporting period (M1 – M9)

During the Phase 1 of the project (M1-M9), WP1 has worked on the following activities within the scope of Task 1.1:

- Definition of use cases: THALIT defined the Obstacle Detection and Avoidance System (ODAS); BOS defined the Intelligent Predictive Cruise Control (PCC).
- Identification of functional and non-functional requirements. When needed, general, high level NFR requirements (fault tolerance, time predictability, energy-efficiency) shall be later split, in order to make them modellable.
- Evaluation of DSML provided by selected SW tools (AMALTHEA for automotive domain, Capella for railway domain) in order to get a clear understanding to what extent the language can model the requirements and what extensions are needed.
- Identification of HW peripherals, such as sensors and boards.
- Where possible, identification of software components such as APIs and libraries.

In Figure 1 the ODAS block diagram is presented. The system is composed by two main subsystems: the Sensor Data Fusion (SDF) and the AI Analytics components. The SDF component will be in charge of collecting a huge mass of raw data from sensors installed in tram vehicle.

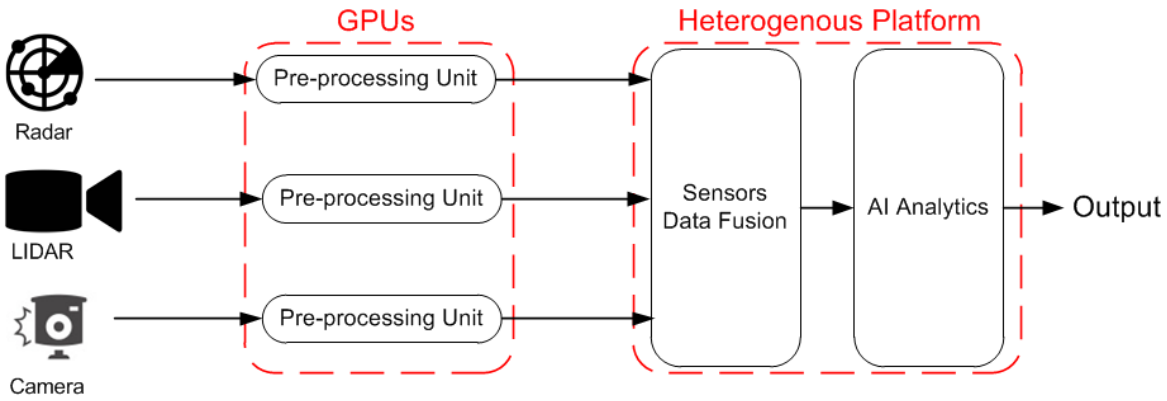

Figure 1. ODAS concepts.

The intelligent *Predictive Cruise Control* (PCC) use case, which is introduced by Bosch, is an example for the increasingly autonomous decision-making capabilities of advanced automotive systems. *Figure 2* shows the overall system-of-systems in which an existing Cyber Physical System (CPS) is enhanced with a new CPS implementing a new advanced functionality. The use case consists of four components: the already existing *Adaptive Cruise Control* (ACC) and the *powertrain control* subsystem, and the new advanced functionalities PCC and *Traffic Sign Recognition* (TSR) subsystem.

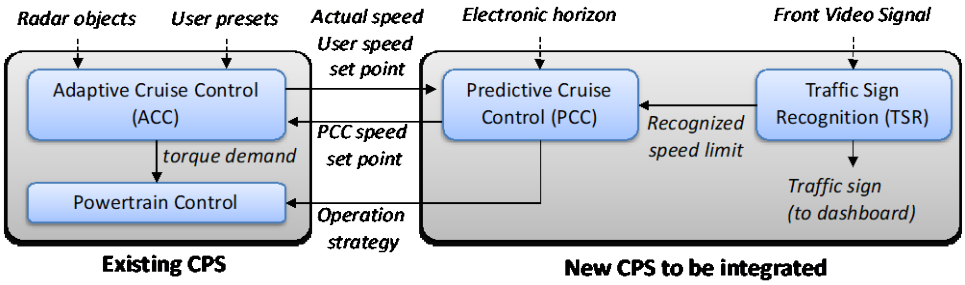

Figure 2: Block diagram of the PCC use-case.

WP1 has worked on the following activities within the scope of Task 1.4:

- SSSA familiarized with the AMALTHEA modelling framework with the help of BOS and started extending an AMALTHEA model provided by BOS to integrate the extensions required to cope with FPGA-based hardware acceleration.

Planned activities until the end of Phase 2 (M10 – M15)

During the Phase 2 of the project (M10-M15), WP1 will work on the following activities

- Single-criterion AMPERE test bench suite definition, including a first analysis of parallel execution on functional safety and cyber-security, and a first release of the meta-model-driven and meta parallel programming abstractions (with WP2).
- Further Analysis of DSMLs, with special focus on the applicability of CAPELLA on the railway use-case.

- Evaluation of functional safety aspects required at each integrity level defined in the safety standards ISO26262, IEC61508, EN 50126, 50128 and 50129, which special interest on the isolation features required by each standard.
- Definition of model-driven extensions.
- SSSA will develop modelling extensions for AMALTHEA to specify hardware acceleration, and will support BSC in investigating extensions to specify concurrency.
- TRT, in collaboration with THALIT, will study the ODAS use case to identify the Capella model extensions required.

3.2. WP2 - Model transformation and code generation

The main objective of WP2, led by BSC, is to enable the efficient transformation of the meta-model-driven abstraction (WP1) into parallel code optimized for achieving maximum performance while keeping the functional and non-functional requirements of the system, including energy, time and fault-tolerance (WP3). To reach this goal, WP2 will:

1. Develop a meta-parallel programming abstraction including the key features of current parallel programming models, and also the functional and non-functional constraints, as well as the tuneable parameters of tensor data computations.
2. Extend parallel programming models to support: (1) the new features included in the meta-parallel programming abstraction, and (2) the new offloading and Dynamic Partial Reconfigurable (DPR) mechanisms (WP4) to efficiently manage heterogeneous computation including CPUs, GPUS and FPGAs.
3. Develop the code synthesis tool that will transform a DSMLs system into parallel code optimized for achieving the maximum performance, considering the multi-criteria optimization phase at analysis time to fulfil non-functional requirements.

Table 3 and Table 4 present an overview of the status of WP2 tasks and the deliverables submitted during the reporting period, respectively.

Table 3. WP2 tasks status overview.

Task	Title	Start Month	End Month	Status
T2.1	Model transformation requirements specification	M1	M7 (delayed)	Completed
T2.2	Meta parallel programming abstraction and parallel programming model extensions	M8	M27	Ongoing
T2.3	Performance-aware transformation techniques	M8	M27	Ongoing
T2.4	Multi-criteria optimization model transformation	M16	M27	Not started
T2.5	Performance-aware model transformation validation	M28	M36	Not started

Table 4. WP2 deliverables submitted during the reporting period.

Delive rable	Title	Lead Benef.	Task	Due month
D2.1	Model transformation requirements specification	M1	T2.1	M7

All WP2 objectives for this period (M1-M9) have been successfully achieved.

Description of progress by partners' contributions during the reporting period (M1 – M9)

During the *Phase 1* of the project (M1-M9), WP2 has worked on the following activities within the scope of Task 2.1:

- BSC has analysed the most advanced parallel programming models (PPMs) for exploiting heterogeneous architectures, including OpenMP, OmpSs, CUDA and OpenCL. The most relevant characteristics of these models are summarized in Table 5 and Table 6. Based on the opportunities offered by the different PPMs, as described in D2.1, OpenMP has been selected.

Table 5. Parallel programming models' comparison based on parallelism patterns and architecture abstraction.

	Parallelism			Architecture abstraction		
Parallel Programming Model	**Data parallelism**	**Asynchronous task parallelism**	**Host/device**	**Abstraction of memory hierarchy**	**Data and computation binding**	**Explicit data mapping host/device**
OpenMP	parallel for simd	task/taskloop	Host and device (target)	OMP_PLACES, teams and distribute	proc_bind	map(to|from|tofrom|alloc)
OmpSs	for	task	Host and device (target/ implements)	ndrange(n, G1,…, Gn, L1,…,Ln)	-	copy_in/ copy_out/ copy_inout/ copy_deps
CUDA	<<<…>>>	Async kernel launch and memcpy, CUDA graphs	Device only	Blocks/threat shared memory	-	cudaMemcpy
OpenCL	kernel	clEnqueTask	Host and device	Work-group and work-item	-	bufferWrite

Table 6. Parallel programming models' comparison based on synchronizations, mutual exclusions, language binding, error handing and tool support.

	Synchronizations			Mutual exclusion	Language library	Error handling	Tool support
Parallel Programming Model	**Barrier**	**Reduction**	**Join**				
OpenMP	barrier	reduction	taskwait	Locks, critical, atomic, single, master	C/C++ and Fortran based directives	cancel	OMPT interface/ Extrae
OmpSs	-	reduction	taskwait	critical, atomic	C/C++ and Fortran based directives	-	Extrae

CUDA	_syncthreads	-	-	atomic	C/C++ extensions	-	NVIDIA profiling tools
OpenCL	work_group barrier	work_group reduction	-	atomic	C/C++ extensions	exceptions	System/vendor tools

- BSC, in close collaboration with BOS and SSSA, have analysed AMALTHEA and the relationship with the selected PPM, OpenMP.

Table 7. Matching components between the AMALTHEA and the OpenMP models.

AMALTHEA	OpenMP
Task	OpenMP program
Runnable	task construct
Runnable offloaded to an accelerator device (e.g., FPGA, GPU)	target construct
Runnable sequencing constraints and data model	depend clause (associated to the task and target constructs)
Preemption strategy supported: Non-preemption, limited-preemption, fully preemption	Preemption strategy supported: Non-preemption, limited-preemption

- BSC has analysed the state-of-the-art of synthetic tools.

The activities reported within the scope of Task 2.1 have been included in deliverable *D2.1 Model Transformation Requirements*, submitted at M7. Due to the delay on TRT activities, the analysis of the capabilities of CAPELLA to model parallelism has not been completed and so they not included in D2.1. However, the analysis already performed with AMALTHEA allows us identifying the elements at the MDE level that we need to focus on. This analysis is currently been conducted within Task 2.2 and will be reported in *D2.2 First release of the meta-parallel programming abstraction and the single-criterion performance-aware component*.

Planned activities until the end of Phase 2 (M10 – M15)

During the Phase 2 of the project (M10-M15), WP2 has worked on the following activities:

- In the scope of Task 2.2, BSC, in collaboration with BOS and SSSA, is developing a complete test case to help defining the meta-parallel programming abstraction. The test case is being defined with AMALTHEA, and will be transformed into C/C++ code, augmented with information about parallel execution and non-functional requirements, by means of a code synthesis tool like APP4MC. Some extensions required in the parallel programming model to define non-functional requirements, like deadlines and priorities, have already been identified. SSSA will deal with the additional attributes in the model needed to support hardware tasks and their associated C/C++ code to be generated on top of the FRED framework.

  TRT is analysing CAPELLA in detail, which seems not to be suitable for model parallelism in the higher level of abstraction. An extension called Tideal seems to be the best candidate to model parallelism and is a prerequisite to some non-functional analysis (e.g, time performance). Further work is being conducted in collaboration with THALIT to specify the missing concepts in this extension in order to reach the appropriate level of modelling for parallelism.

- In the scope of Task 2.3, BSC has started to work with the platforms selected for the project, as defined in *D5.1 Reference parallel heterogeneous hardware selection*: the Xilinx Zynq UltraScale+ MPSoC

ZCU102 Evaluation Kit and the NVIDIA Jetson AGX Xavier Development Kit. The Nanos runtime, supporting OpenMP and OmpSs, is being analysed for exploiting performance on the heterogeneous system.

3.3. WP3 - Multi-criteria optimization

The main goal of WP3 is to investigate and provide a set of analyses, which are able to perform a multi-criteria optimization at development phase, guiding the model-driven to programming model transformation and ensuring that non-functional constraints (energy efficiency, real-time response and resiliency) are fulfilled, and devise execution models and methods to guarantee their fulfillment at run-time, considering the underlying runtimes and platforms. To reach this goal:

- In what respects to energy-efficiency, WP3 will (i) investigate the energy consumption components present in the selected parallel platform(s) and how are impacted by the different power management knobs and run-time decisions; (ii) devise methods to extract information on (1) workload specification, (2) non-functional constraints included in the parallel programming model and (3) hardware platform characteristics impacting on energy; and (iii) develop energy-aware execution models based on previous information that push the selected parallel platform(s) introspection capabilities beyond what is currently feasible.
- With respect to time predictability, WP3 will (i) investigate and develop predictable execution models of the selected parallel platforms to simplify timing and schedulability analysis, including optimizations in the placement of functionality into cores, offloading operations, DPR operations and computation on accelerators; and (ii) develop timing and schedulability analyses for the proposed scheduling algorithms and heterogeneous execution models developed in WP4.
- With respect to fault tolerance, WP3 will improve the system's fault tolerance, considering reliability and availability aspects resulting in improved system's dependability.

Table 8 and Table 9 present an overview of the status of WP3 tasks and the deliverables submitted during the reporting period, respectively.

Table 8. WP3 tasks status overview.

Task	Title	Start Month	End Month	Status
T3.1	Multi-criteria optimisation requirements specification	M1	M9 (delayed)	Completed
T3.2	Energy Optimisation Strategies	M10 (delayed)	M27	Not Started
T3.3	Predictable Execution Models	M10 (delayed)	M27	Not Started
T3.4	Resilient software techniques	M10 (delayed)	M27	Not started
T3.5	Multi-criteria optimisation validation	M28	M36	Not started

Table 9. WP3 deliverables submitted during the reporting period.

Delive rable	Title	Lead Benef.	Task	Due month
D3.1	Multi-criteria optimization requirements	ISEP	T3.1	M9 (delayed)

As noted in the tables, the activities in WP3 have been delayed, due to the delay in ISEP activities related to the COVID-19 situation. All WP3 objectives for the period have been successfully achieved, at the end of the postponed MS1 (M9).

Description of progress by partners' contributions during the reporting period (M1 – M9)

During the Phase 1 of the project (M1-M9), WP3 has worked on the following activities within the scope of Task 3.1:

- ETHZ, ISEP and BSC have analysed the constraints emanating from use cases, modelling and programming models, runtimes and platforms, identifying and consolidating the set of requirements put forth related to energy-efficiency, real-time behaviour, and resilience.
- SSSA is investigating on the use of deadline-based scheduling for real-time tasks on top of non-symmetric multi-processor platforms, and associated admission control techniques, with a focus on soft real-time guarantees that can be guaranteed on Linux trading off deadline misses for energy efficiency. Preliminary results have been obtained in simulation only and will be included in D3.2 due on PM15.
- ETHZ focused on characterizing the hardware of the platforms identified by WP5 and modelling of energy use. To this end, ETHZ has devised models to allow tracking the energy usage based on linear models by tracking hardware events (e.g., performance counters).
- BSC focuses on applying fault-tolerant software techniques taking benefit of the meta-parallel programming model represented as a DAG. Concretely, the identification of the parallel entities and synchronization mechanisms within the DAG allow to provide fine-grain fault-tolerant techniques applied to a subset of parallel entities or synchronization points where the impact of check-pointing is minimised (e.g., at barriers).

The activities reported within the scope of Task 3.1 have been included in deliverable D3.1 Multi-criteria optimization requirements, submitted at M9.

Planned activities until the end of Phase 2 (M10 – M15)

During the Phase 2 of the project (M10-M15), WP3 will work on the following activities:

- In the scope of Task 3.2, ETHZ, in collaboration with BSC and ISEP will develop efficient resource management strategies (considering heterogeneous hardware resources and associated offload mechanisms) for optimizing the energy efficiency of the system, independently of other non-functional constraints.
- In the scope of Task 3.3, ISEP, in collaboration with BOS, SSSA, BSC and ETHZ will devise execution models that jointly consider the allocation of processing, both at the host and accelerator, and memory and on-chip network resources, with the appropriate timing and schedulability analysis approaches.
- In the scope of Task 3.3, SSSA will continue investigating on adaptive statistics-based approaches to ensure that the amount of deadline misses of soft real-time tasks can be kept under control via on-line monitoring and dynamic adaptation of the scheduling parameters. The focus will be on scenarios where multiple tasks may have inter-dependencies composing a real-time DAG to be activated with a

minimum inter-arrival period. The approach will consider also possible calls to GPU or FPGA accelerated functions. SSSA will also continue the analysis of the DNN inference frameworks, select one to be used as a reference for the project, and start building an analytical model to be validated via profiling of the actual accelerators.

- In the scope of Task 3.4, BSC, in collaboration with ISEP, THALIT and ETHZ will design approaches to support redundancy (modular redundancy techniques) to support fault-tolerance requirements.

The work in phase 2 of the project will consider each one of the non-functional requirements (energy-efficiency, real-time behaviour and resilience) independently. The multi-criteria optimization phase (phase 3) will then take into account all these effects to devise the best-combined solutions.

3.4. WP4 - Run-time Parallel Framework

The main objective of WP4, led by SSSA, is to provide run-time support for low-energy computing, time predictability, fault tolerance, and safety/security, as well as for efficient hardware acceleration. To reach this goal, WP4 will:

1. Investigate and develop novel mapping and scheduling techniques to allow a proper management of platform resources, with the optimizations provided by WP3, and so that the requirements provided by WP1 are fulfilled.
2. Develop low-intrusive monitoring mechanisms for timing and resource access characterization and investigate and develop software resilient solutions to complement hardware modular redundancy techniques supported in parallel processors.
3. Investigate and develop run-time mechanisms for managing dynamically-configurable FPGA hardware accelerators with support for efficient synchronization and dynamic adaptation to maximize (and guarantee) non-functional constraints devised in WP3.

Table 10 and Table 11 present an overview of the status of WP4 tasks and the deliverables submitted during the reporting period, respectively.

Table 10. WP4 tasks status overview.

Task	Title	Start Month	End Month	Status
T4.1	Run-time requirement specification	M1	M7 (delayed)	Completed
T4.2	Run-time Energy Support	M7	M27	Ongoing
T4.3	Run-time for predictable parallel heterogeneous computing	M7	M27	Ongoing
T4.4	Run-time resilience methods	M7	M27	Ongoing
T4.5	Run-time mechanisms for safety/security	M7	M27	Ongoing
T4.6	Run-time validation	M28	M36	Not started

Table 11. WP2 deliverables submitted during the reporting period.

Delive rable	Title	Lead Benef.	Task	Due month
D4.1	Run-time Architecture	SSSA	T4.1	M6

All WP4 objectives for this period (M1-M9) have been successfully achieved.

Description of progress by partners' contributions during the reporting period (M1 – M9)

WP4 has worked on the following activities within the scope of Task 4.1:

- SSSA specified the requirements for the OS and the run-time support for predictable execution on heterogeneous platforms with FPGA-based hardware acceleration. Applications have been specified in terms of software (to be executed on processors) and hardware tasks (to be executed on FPGAs). Technological requirements have been formalized for hardware tasks, especially concerning run-time reconfiguration and allocation issues and hardware-related components. Execution behavior and scheduling issues for software tasks have also been formalized. The requirements also include the list of operations that shall be possible to perform via the API offered by AMPERE to handle acceleration requests.
- ETHZ has explored the hardware platforms selected as part of WP5 from an energy-efficiency standpoint, and identified hardware events, tuning knobs and parameters that can be monitored or managed from software. Based on this, ETHZ has determined which requirements that are posed to the AMPERE runtime system to perform low-overhead monitoring and actuation of the commercial platforms for achieving energy-efficient execution.
- In cooperation with the other partners involved in the work package, SSSA consolidated the structure of the overall run-time architecture of AMPERE. A possible instance of the AMPERE run-time architecture is illustrated in Figure 3 while a detailed description is reported in D4.1.

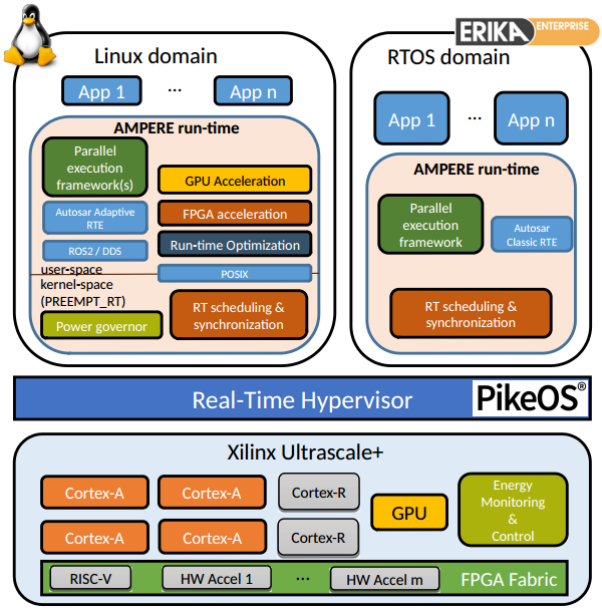

Figure 3 - Possible instance of the AMPERE run-time architecture.

WP4 has worked on the following activities within the scope of Task 4.2:

- ETHZ has started developing an efficient implementation for the energy monitoring scheme that is able to meet the low-overhead requirements for the AMPERE runtime, in particular on the NVIDIA platform.

WP4 has worked on the following activities within the scope of Task 4.3:

- SSSA has started studying the Xilinx Ultrascale+ and the novel Xilinx FPGA Mananger to the purpose of developing the run-time support for DPR FPGAs. SSSA has also started analysing the major frameworks for accelerated DNN inference on FPGA (DNNDK, CHaiDNN, and FINN).
- SSSA and ETHZ identified an interesting terrain for collaboration in the context of Task 4.2, for designing appropriate low-overheads energy-modeling strategies, aimed at supporting energy-aware scheduling of real-time workloads on non-SMP platforms.

Planned activities until the end of Phase 2 (M10 – M15)

The following activities are expected to be carried out in the coming months:

- SSSA will continue the development of the run-time support for DPR FPGAs on the Ultrascale+ platform aiming at a seamless integration with the Xilinx FPGA Manager to facilitate the final deployment and increase the impact and portability of the realized solution.
- SSSA will continue the analysis of the DNN inference frameworks, select one to be used as a reference for the project, and investigate on the modifications required to handle the corresponding accelerators within the AMPERE eco-system.
- SSSA plans, in conjunction with ETHZ, to analyze and profile the power consumption of the Ultrascale+ board selected in T5.1, when executing a variety of workloads imposing different levels of stress on the various elements of the internal CPU architecture, as well as when performing calls to accelerated GPU/FPGA functions. SSSA will investigate on how to integrate in the best possible way the energy model coming out of this profiling activities with the dynamic run-time mechanisms to be realized in WP5, and the platform optimization needed in WP3.
- ETHZ will implement runtime mechanisms and policies for power/energy monitoring and actuation, within the scope of the AMPERE runtime, based on the monitoring and management mechanisms identified, and in coordination with the offline optimization for energy-efficiency in WP3.

3.5. WP5 - Operating system and parallel platforms

The main objective of WP5, led by EVI, is the design and development of the operating system and hypervisor for the selected reference platforms.

Table 12 and Table 13 present an overview of the status of the WP5 tasks and the deliverables submitted during the reporting period, respectively.

Table 12. WP5 tasks status overview.

Task	Title	Start Month	End Month	Status
T5.1	Platform selection	M1	M6	Completed
T5.2	General-purpose operating system	M7	M27	On-going
T5.3	Real-time operating system	M7	M27	On-going
T5.4	Hypervisor	M7	M27	On-going
T5.5	Operating systems & hypervisor validation	M28	M36	Not started

Table 13. WP5 deliverables submitted during the reporting period.

Delive rable	Title	Lead Benef.	Task	Due month
D5.1	Reference parallel heterogeneous hardware selection	SYS	T5.1	M6

Description of progress by partners' contributions during the reporting period (M1 – M9)

During the first 6 months, all partners have collaborated in Task 5.1 for selecting the most suitable reference hardware platform to be used in the project. This activity has included a survey of the characteristics of the potential platforms available on the market. Partner SYS has collected all this information in deliverable D5.1. As illustrated in such deliverable, this process resulted in the selection of the Xilinx Ultrascale+ ZCU102 and the NVIDIA Jetson AGX Xavier boards.

Then, partners SYS and EVI started the activity for porting the hypervisor and the operating system on the Xilinx ZCU102 platform:

- In Task 5.2, EVI ported the PREEMPT_RT patch on the Linux BSP provided by Xilinx for the reference platform.
- In Task 5.4, SYS has ported the PikeOS kernel with basic BSP support on Xilinx UltraScale+. SYS is currently waiting the requirements from the other partners to finalize the development of the full BSP/PSP.
- Additionally, SYS has ported the OpenMP framework on PikeOS, with a few limitations for PikeOS Native applications (i.e. no thread deletion, no automatic load balancing, no dynamic change of the number of available threads).
- SSSA started development of adaptive dynamic partitioning strategies for SCHED_DEADLINE, as investigated in simulation only in WP3; these developments are preliminarily being carried out on x86 architectures for ease of testing and debugging, but they will be extended with integration with the energy-awareness features of Arm architectures in a short future.

Planned activities until the end of Phase 2 (M10 – M15)

In the coming months, SYS and EVI will continue the activity for porting PikeOS, Linux and ERIKA RTOS on the ZCU102 platform. A preliminary version will be released at M15 in the Deliverable D5.2.

In particular:

- Partner SYS will provide the PikeOS hypervisor and the Linux BSP for the Xilinx platform
- Partner EVI will then port the ERIKA Enterprise RTOS on the hypervisor and integrate the PREEMPT_RT patch on the Linux BSP provided by SYS
- EVI will also start implementing a version of its RTOS for the RISC-V architecture (meant to be run on the Ariane soft-core, synthesized on the FPGA by ETHZ).
- SSSA plans to realize the energy-aware EDF-based scheduler under investigation in the context of WP3 in simulation, in the Linux kernel by enhancing the SCHED_DEADLINE code base, by leveraging the Energy-Aware Scheduling (EAS) framework within the kernel for Arm processors. SSSA plans to use the PREEMPT_RT patch by EVI mentioned above, as well as the adaptive partitioning strategies under development, as starting points for this work.

3.6. WP6 - AMPERE System Design and Computing Software Ecosystem Integration

The main objective of WP6, led by TRT, is the integration of the software components of the AMPERE software ecosystem and the verification of the whole ecosystem according to use cases defined in the project.

Table 14. AMPERE system design and computing ecosystem integration.

Task	Title	Start Month	End Month	Status
T6.1	AMPERE ecosystem requirement specification	M1	M15	On-going
T6.2	Synthesis tool integration	M7	M27	Not started
T6.3	Integration of run-time/OS mechanisms	M7	M27	Not started
T6.4	Integration of the AMPERE's technology into use case environments	M16	M36	Not started

Table 15. WP6 deliverables submitted during the reporting period.

Delive rable	Title	Lead Benef.	Task	Due month
D6.1	AMPERE ecosystem requirements and integration plan	BSC	6.1	M7 (delayed)

Description of progress by partners' contributions during the reporting period (M1 – M9)

During the Phase 1 of the project (M1-M9), WP6 has worked on the following activities within the scope of Task 6.1:

- All partners have collaborated in the definition of the software components and tools that will form the AMPERE ecosystem. Figure 4 depicts this ecosystem, identifying the initial set of software components that form it, and their relationships. Additionally, Table 16 describes the ownership and licensing characteristics of the software components. These components will be revised (and updated, if needed) in *D6.2 Refined AMPERE ecosystem interfaces and integration plan*.
- All partners have collaborated to define the interface between the different components, as described in D6.1.
- BSC, with the revision and agreement of all partners, has defined an integration plan including the processes, tools and guidelines for a smooth integration. Figure 5 shows integration process of different components of the AMPERE ecosystem, as defined in D6.1.
- BSC has created the needed cooperative development tools to ensure the communication between partners and the integration of the different components is smooth. These tools include a Slack channel, a Git repository and an Intranet.

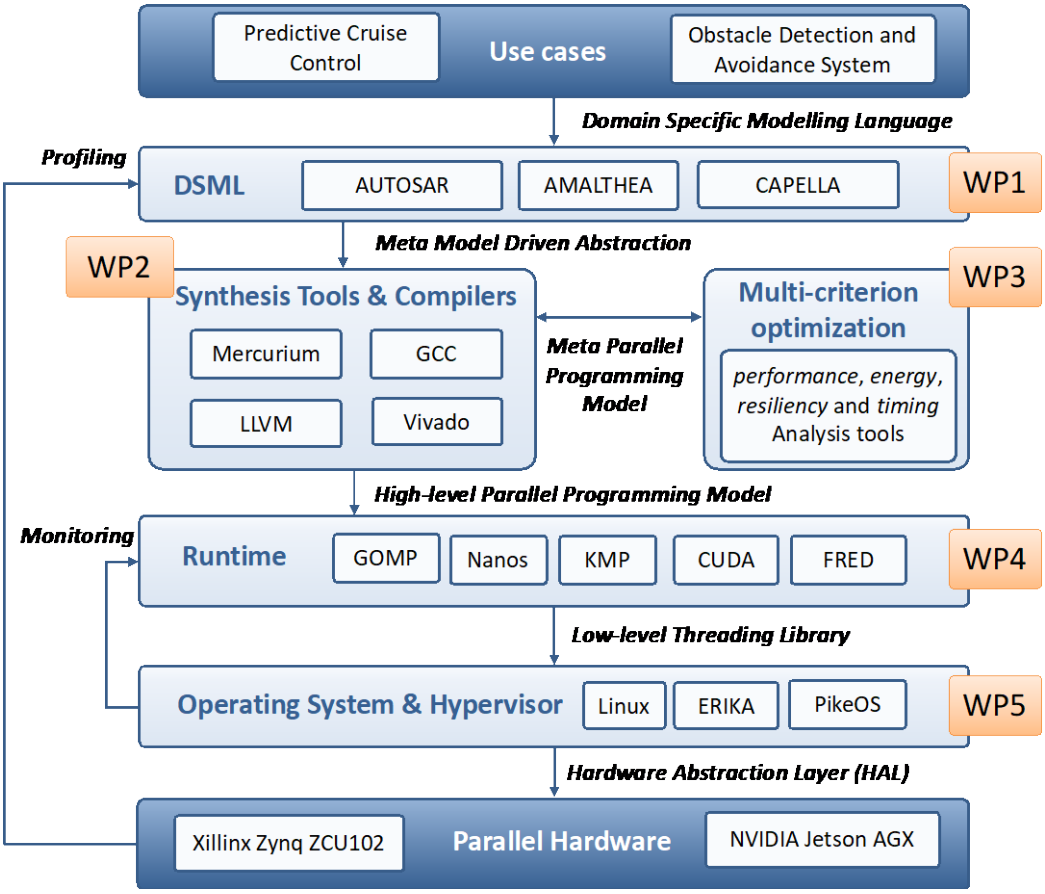

Figure 4. AMPERE Software development ecosystem: components, relationships and interfaces.

Table 16. Initial selection of AMPERE software components at MS1.

Software Layer / WP	Software component	WP	Owner	License
Domain Specific Modelling Language (DSML)	AUTOSAR	WP1	AUTOSAR	Proprietary
	AMALTHEA		BOS	Open source
	CAPELLA		TRT	Open source
Artificial Intelligence	TensorFlow	WP1	Google	Open source
Parallel Programming Models	OpenMP	WP2	OpenMP	Open source
	CUDA		NVIDIA	Proprietary
Compilers and Hardware Synthesis Tools	Mercurium	WP2	BSC	Open source
	GCC		GNU	Open source
	LLVM		LLVM	Open source
	Vivado		Xilinx	Proprietary
Analysis and Testing Tools	Multi-criteria Analysis and Testing Tools	WP3	AMPERE	Open source
Runtime Libraries (RTL)	GOMP	WP4	GNU	Open source
	Nanos		BSC	Open source
	KMP		LLVM	Open source

	Fred		SSSA	Open source
Operating Systems	Linux	WP5	Linux	Open source
	ERIKA Enterprise		EVI	Open source
Hypervisors	PikeOS		SYS	Proprietary

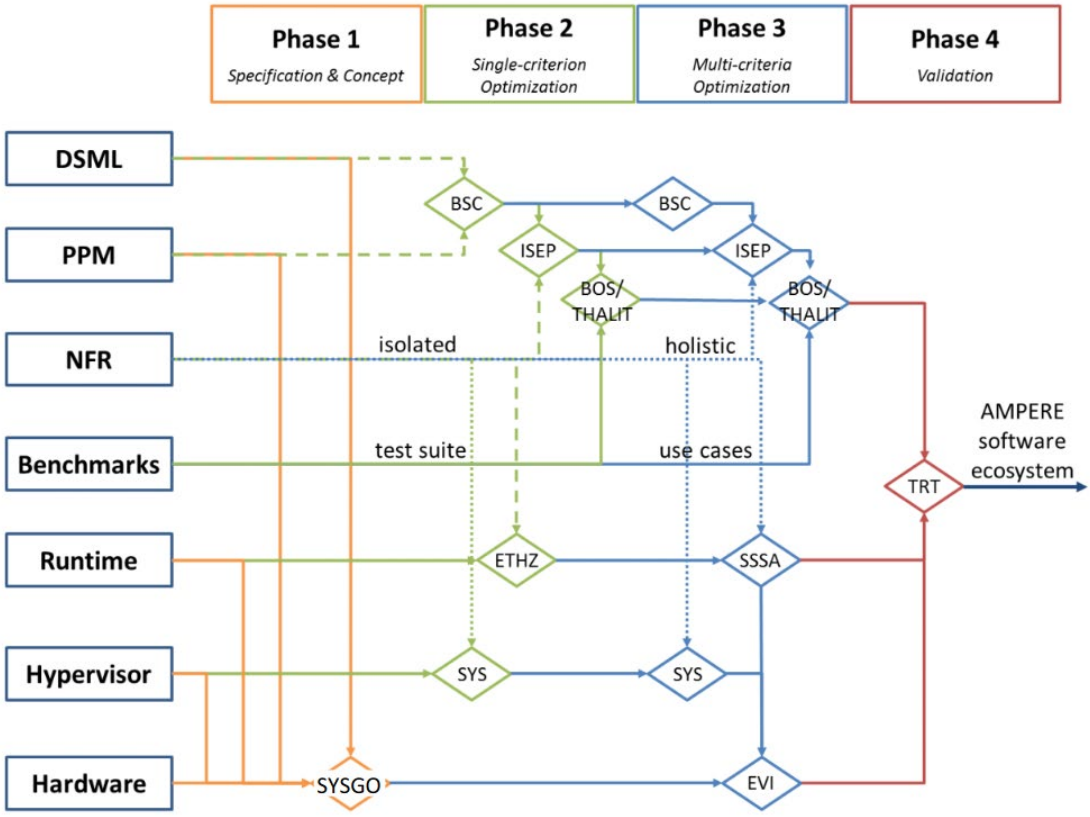

Figure 5. Tree-like diagram of the integration of the AMPEREecosystem component.

Planned activities until the end of Phase 2 (M10 – M15)

During the Phase 2 of the project (M10-M15), WP2 has worked on the following activities:

- In the scope of Task 6.1, BSC is working on extending the integration platform with an issue tracking tool (Gitlab) and a continuous integration system (Gitlab or Jenkins).
- In the scope of Task 6.2 and Task 6.3, BSC, in collaboration with all partners, aims to work towards the integration of the different software components, using the methods stablished in Task 6.1.

3.7. WP7 - Communication, Dissemination and Exploitation

Performed work

During the first 9 project months, the WP7 team has established the project's image with appropriate branding, templates, and dissemination material. The project's website was launched on 10 June 2020 and has been enriched with updates, news, and details on the IAB and use cases. In addition, the consortium participated in a total of 8 events disseminating the project. The press coverage was achieved for this year with 1* press release and several press articles that resulted in 12** press clippings. With the aim to raise awareness about the project and its results, update key stakeholders on project progress and build a

community around the project, the WP7 team has been posting regular updates on the project's dedicated LinkedIn and Twitter channels.

The WP7 has also successfully submitted the following deliverables:

- Communication and Dissemination: D7.1 Communication and Dissemination Plan (M3).

Results and Future Plans

The Table 17 and brief explanations below demonstrate the current status of the communication and dissemination KPIs:

Table 17. Status of the communication and dissemination KPIs.

Key performance indicator	Explanation	Achieved (M1-M9)	Total target (M36)
Scientific Publication	Papers published in scientific venues and journals	3 publications	At least four publications per year
Academic and Industrial Events	• Participation in events • Events organized, including conference booths, tutorials and workshops (with significant attendance, i.e. above 30 people)	• 8 participations in events • n/a	• At least 10 participations • At least one event organized and a booth in smart mobility related event
Press Strategy	• Number of press releases • Press clippings	• 1* press release • 12** press impacts	• One press release per year • At least 25 press impacts
Whitepapers and Factsheet	Number of business and scientific whitepapers or factsheets published	n/a	At least one business and one scientific whitepaper or factsheet
Website	Visitor statistics (number of unique website visitors and their location captured by Google Analytics)	• 382 unique users	At least 1000 unique visitors per year
Social Media Channels	• Number of followers in Twitter • Number of Linkedin followers	• Twitter: 95 followers • Linkedin: 118 followers	• At least 250 over the project • At least 150 over the project
Dissemination Materials	• Number of posters • Number of project videos	• One poster • n/a	• At least two posters • At least two videos

Website sessions: The website was launched at the beginning of June 2020. Due to the Covid-19 lockdown, the website development (design + programming + consortium approval) had a delay of two months. New content has been created and added continuously specifically to populate the website with news, information about use cases and the Industrial Advisory Board (IAB) as well as new press clippings and more social media engagement. These efforts are on-going. More technical related content will be developed in the coming months once the project gets results and more publications.

Press releases: A first press release was published at the beginning in order to announce the project launch and a second one will be launched at the beginning of 2021 to provide some information about the project's

progress. A final one will be produced at the end of the project demonstrating the project's achievements and complete picture.

Press clippings: AMPERE has had a good press impact in technical media outlets such as HPC Wire, eeNews, News break, Primeur Weekly Magazine and L'Embarque. The consortium posted a blog that can be an excellent opportunity to drive through leadership, awareness, and credibility, since each year blogs receive more than 200,000 page views on average. Moreover, AMPERE was featured on a podcast that can position the project's technology more than regular channels such as radio. More news articles will be generated to be shared with similar press channels.

Whitepaper and factsheets: No whitepaper or factsheet has been produced up to this point, as these will be created towards the end of the project summarizing the scientific results, software integration, and use case applications.

Events and conferences attended: The events where AMPERE experts participated during the reporting period reached 7 in total. Several presentations, demos, and booths were held in international conferences and exhibitions, such as DATE, ISC, ISORC, SCOPES, ECTRS, and LCTES. More events are planned for the following months in order to present the project's results. The attendance to physical events might be affected due to the Covid-19 pandemic but it will be replaced by its presence on online events, whenever applicable.

Scientific publications: Three scientific publications have been reported so far. This number will increase as the project produces scientific results. WP7 sent specific guidelines to inform AMPERE partners about the EC requirements on publications and Open Access. More publications will be published in the future and regularly updated on the project website. It is noteworthy to mention that AMPERE partners already published a joint (vision) paper involving all the partners, at IEEE ISORC 2020, and are extending the work to submit it to a special issue of the Elsevier JSA journal.

Social media: Twitter scientific and academic followers have been increasing periodically. The editorial plan and news pieces published on the website along with the efforts for more press coverage and the new AMPERE webpage have helped to engage many more members on Twitter. The number of LinkedIn followers has also increased due to the enriched project website and press impact. WP7 will keep working on growing our social media followers and engagement.

Project posters: A generic poster with the overview of the project has been created. A second, updated poster will be created at a later stage once the project has produced more solid scientific results.

Project videos: No project video has been produced up to this point, as these will be created once there is progress to display in an audiovisual form. Two videos are planned for the next stages of the project to explain the technology and scientific results.

Flyer and project overview presentation: A flyer and a project overview presentation have been created to be used in presentations and events that AMPERE partners attend and participate in.

3.8. WP8 - Management

Main objectives of WP8 are: 1) continuous monitoring to deliver Project objectives 2) ensuring clear and effective communication between partners, 3) establishing and reinforcing effective management and quality procedures and 4) providing operational management support. Actions implemented as part of WP8 tasks described below have been implemented with participation and collaboration of all AMPERE partners.

Table 18 and Table 19 present an overview of the status of WP8 tasks and the deliverables submitted during the reporting period, respectively.

Table 18. WP8 tasks status overview.

Task	Title	Start Month	End Month	Status
T8.1	Administrative and financial management	M1	M36	On-going
T8.2	Project coordination	M1	M36	On-going
T8.3	Internal Communication, Quality and Risk management	M1	M36	On-going

Table 19. WP8 deliverables submitted during the reporting period.

Deliverable	Title	Lead Benef.	Task	Due month
D8.1	Project management plan and quality guidelines	BSC	8.1, 8.2, 8.3	M3
D8.2	Project management and collaboration tools	BSC	8.3	M3
D8.3	Data Management Plan DMP	BSC	8.3	M6
D8.4	Progress report for the technical review	BSC	8.1	M9

Task 8.1 Administrative and financial management

BSC has organized Kick Off Meeting at own premises on 27th - 28th of January 2020. Besides having technical discussions, the consortium was introduced to the project day-to-day operational management and reporting to the European Commission. All partners were represented by at least one member with a total of 27 attendees. The same occasion was used to organize first meeting with the Industrial Advisory Board members on the 29th of January 2020 and to get their opinion and advise on the best course that the project should take to maximize opportunities for future exploitation of the results.

The First AMPERE Project Meeting was organized by BSC as a virtual event by using Zoom videoconferencing software, due to COVID-19 provoked restrictions in mobility. All partners were represented by at least one member with a total of 26 attendees. Each partner had usual time for presenting their progress as in a regular F2F meeting. To ease long periods of attention needed, the meeting was organized in hour and a half sessions twice a day during four consecutive days.

BSC organizes monthly teleconferences of the General Assembly (GA) which also use Zoom videoconferencing tool. The meeting minutes are made available on the project intranet.

BSC has appointed internal consortium reviewers of each deliverable to be presented during the project. So far, eleven deliverables (Table 20) were presented and BSC has followed-up their preparation and review process.

Table 20. Deliverables of AMPERE presented in the period M1-M9.

Deliverable #	Deliverable name	Lead. name	Reviewer	Delivery date
D1.1	System models requirement and use case selection	THALIT	BOS	15/09/20
D2.1	Model transformation requirements	BSC	SYS	03/08/20
D3.1	Multi-criteria optimization requirements	ISEP	THALIT	30/09/20
D4.1	Run-time Architecture	SSSA	EVI	05/08/20
D5.1	Reference parallel heterogeneous hardware selection	SYS	BSC	03/08/20
D6.1	AMPERE ecosystem requirements and integration plan	BSC	THALIT	05/08/20
D7.1	Communication and Dissemination Plan	BSC	ETHZ	30/03/2020
D8.1	Project management plan and quality guidelines	BSC	TRT	30/03/2020
D8.2	Project management and collaboration tools	BSC	SSSA	30/03/2020
D8.3	Data Management Plan (DMP)	BSC	SSSA	30/06/2020
D8.4	Progress report for technical review	BSC	THALIT	Expected 08/10/2020

WP8 elaborated four deliverables (including this progress report).

Deliverables D8.1 and D8.2 were written and submitted in month three of the project execution.

D8.1 “Project management plan and quality guidelines” is meant to facilitate the day-to-day management of the project, providing an overview of the management and administrative procedures of the project and ensuring that all participants in AMPERE understand the structure of the project, the different responsibilities related to each role in the management structure and the main legal documents of reference. It also defines the internal procedure for the submission of Deliverables and Periodic Reports. The deliverable will be updated during the life of this project, if necessary.

D8.2 “Project management and collaboration tools” explains collaboration tools which were created by BSC to facilitate the consortium communication and exchange of documents.

In month six, D8.3 “Data Management Plan DMP” was submitted to describe the main elements of the data management policy that will be used with regard to all the datasets generated by this project, according to the Guidelines on Data Management in H2020. The deliverable will be updated during the life of this project, if necessary.

The coordinator and the Project Officer have effective communication and any delay in presenting deliverables has been notified. Key points of the communications are shared with the consortium.

A Consortium Agreement (CA) based upon a DESCA Model CA was negotiated and agreed with the partners. In addition to the Project Grant Agreement, the CA defines the responsibilities of the partners, the liability, the management structure, rules for decision-making and conflict solving, financial provisions and payments as well as the IPR.

With the support of the AMPERE Project Officer, first amendment to the Grant Agreement was presented with the changes described in the section 7.1.

BSC distributed the pre-financing payment according to the Grant Agreement. Table 21 shows the distribution of the pre-financing and the foreseen payments to partners.

Table 21. AMPERE budget and payments.

Partner	Budget Annex I	EC Contribution	Pre-financing 75%	Guarantee fund 5%	Rest 20%
BSC	707.500,00 €	707.500,00 €	530.625,00 €	35.375,00 €	141.500,00 €
ISEP	326.250,00 €	326.250,00 €	244.687,50	16.312,50 €	65.250,00 €
ETHZ	497.750,00 €	497.750,00 €	373.312,50€	24.887,50 €	99.550,00 €
SSSA	464.375,00 €	464.375,00 €	348.281,25€	23.218,75 €	92.875,00 €
EVI	496.250,00 €	496.250,00 €	372.187,50€	24.812,50 €	99.250,00 €
BOS	499.372,50 €	499.372,50 €	374.529,38€	24..968,62 €	99.874,50 €
TRT	723.630,00 €	723.630,00 €	542.722,50 €	36181,50 €	144726,00 €
THALIT	573.125,00 €	573.125,00 €	429.843,75 €	28.656,25 €	114.625,00 €
SYS	711.175,00 €	711.175,00 €	533.381,25 €	35.558,75 €	142.235,00 €
		4.999.427,50 €	**3.749.570,625 €**	**249971,375 €**	**999.885,50 €**
			4.999.427,50 €		

In accordance with AMPERE DoA, BSC prepared internal use of resources report in month six to compare project progress and timeline with usage of the available funds, a way to monitor correct implementation of the project. The report has revealed some underspending, mainly due to delays in personal recruitment because of COVID-19 situation. The current status of the AMPERE use of PMs can be found in the section 8.

Task 8.2. Project coordination

The project coordination deals with the strategic and technical management of progress of WPs. It is based on regular meetings between the coordinator and the General Assembly, while specific WP meetings are scheduled on a demand. Decisions taken in the meetings are described in the minutes available to whole consortium in the project intranet.

Task 8.3. Internal Communication, Quality and Risk management

To facilitate internal consortium communication, different email distribution lists have been created: AMPERE (for general project communications), AMPERE-ga (for General Assembly relevant communications) and AMPERE-tech (for technical discussions), AMPERE-diss (for the project dissemination activities). In addition, the project's email was created (ampere-project@bsc.es) and appears on the website under the contact section. It offers website's visitors or users a channel to communicate with the AMPERE consortium.

An internal workspace at Slack has been created to share project news and documents in a fast way.

Zoom Video Communications services is used for remote conferencing for General Assembly monthly meetings and for any technical meeting if needed. So far, First Project Meeting in July 2020 was organized by using Zoom.

To provide the access of the consortium to the project documentation, BSC created a password-protected intranet hosted on the project website (www.ampere-euproject.eu). BSC is uploading all relevant documents which include: legal documents (Description of Action, Grant Agreement, amendment, Consortium Agreement); meetings minutes and presentations; dissemination material (templates, logos etc.), final versions of deliverables and dissemination documents (papers, posters etc.). For collaborative contribution of all consortium to working versions of the documents, AMPERE GitLab project instance has been created. It also contains a repository for software related to the development of the AMPERE software architecture.

BSC has monitored the preparation of deliverables by setting a calendar for the author/s and internal consortium reviewer/s. First draft ready for the review process is made available to the reviewer 21 days before the deadline. The reviewer has 7 days to provide comments and suggestions for the improvement which the author needed to implement until five days before the deadline. The new, consolidated version of the author so far has always been accepted by the reviewer, as the comments were reflected in it. The Project Coordinator also needs to give his approval before the final version of the deliverable is submitted to the Funding and Tenders Portal.

Quality assurance and risk assessment procedures were established as described in D8.1. The risks are monitored on the monthly teleconferences and every six months. Currently, none of the risk foreseen in DoA has materialized.

COVID-19 outbreak related unforeseen risks are being followed on the monthly teleconferences and in a shared document where updates are reported. More details of COVID-19 provoked risks can be found in section 7.2.

During the confinement period in different countries, all beneficiaries kept working remotely. Still, the following difficulties were detected:

- recruitment processes at BSC, ISEP and SSSA were affected;
- BOS, TRT and THALIT have experienced partial stop of activities in certain periods;
- spanning from April 2020 to June 2020, THALIT reduced working time of personnel in a range from 1-day to 3-days a week;
- spanning from April 2020 to June 2020, THALIT requested personnel to have forced leaves in a range from 1-day to 3-days a week;
- starting from July SYSGO GmbH has reduced working time of personnel to 4-days a week;
- there was a delay in shipping necessary equipment;
- there are difficulties of working from home related to having persons in charge.

As a consequence, majority of M6 deliverables had 1-3 months delay and part of beneficiaries reported less PMs than it was initially planned (as described in section 7). The consortium is overcoming the risks with higher involvement of available personnel (even during forced stops of activities), while the new personnel for SSSA has now already been recruited. If needed, unused personnel efforts could be used in greater extent later on along the project course.

Planned activities until the end of Phase 2 (M10-M15)

According to AMPERE Gantt chart included in the Description of Action, the consortium has completed the Phase 1 (M1-M6) and entered into Phase 2 (M7-M15), by submitting all the deliverables and achieving the MS1. WP8 will continue to monitor the work of the project through monthly GA meetings and bi-annual face-to-face whole consortium meetings.

4. Update of the plan for exploitation and dissemination of result

Not applicable.

5. Update of the data management plan

Not applicable.

6. Deviations from Annex 1 and Annex 2

6.1. Amendment

The consortium presented the Amendment AMD-871669-2 including the following changes to the Grant Agreement:

1. Addition of "Instituto Politécnico do Porto" (IPP) as Third Party free of charge of beneficiary ISEP. IPP's contribution is in WP2, WP3 and WP8 (see Table 22 and 23).

Table22. AMPERE total effort (PMs) of ISEP.

	WP1	WP2	WP3	WP4	WP5	WP6	WP7	WP8	TOTAL
PMs DoA ISEP	2	12	30	12	0	6	2	1	65
PMs ISEP	2	**11**	**28**	12	0	6	2	**0.5**	61.5
PMs IPP	0	**1**	**2**	0	0	0	0	**0.5**	3.5

Table 23. AMPERE total budget of ISEP.

	Direct personnel costs	Other direct costs	Direct cost of subcontracting	Indirect costs	Total
Budget DoA ISEP	227.500€	33.500€	0	65.250€	326.250€
New budget	227.500€	33.500€	0	65.250€	326.250€
- ISEP	209.500€	33.500€	0	60.750€	303.750€
- IPP	18.000€	0	0	4.500€	22.500€

2. Addition of SYSGO GmbH as Linked Third Party of beneficiary SYSGO SRO. SYSGO GmbH contributes in all WPs in which SYSGO SRO participates (Table 24) with cost of 182.157€ (Table 25).

Table 24. AMPERE total effort (PMs) of SYSGO.

	WP1	WP2	WP3	WP4	WP5	WP6	WP7	WP8	TOTAL
PMs DoA SYSGO SRO	3	4	0	8	30	15	3	1	64
PMs SYSGO SRO	**2**	**3**	0	**6**	**22**	**10**	**1**	**1**	45
PMs SYSGO GmbH	**1**	**1**	0	**2**	**8**	**5**	**2**	**0**	19

Table 25. AMPERE total budget of SYSGO.

	Direct personnel costs	Other direct costs	Direct cost of subcontracting	Indirect costs	Total
Budget DoA SYSGO SRO	461.440€	59.500€	60.000€	130.235€	711.175€
New budget	461.440€	59.500€	60.000€	130.235€	711.175€
- SYSGO SRO	324.450€	53.000€	60.000€	91.568€	529.018€
- SYSGO GmbH	136.990€	6.500€	0	38.667€	182.157€

3. Addition of "University of Siena" (UNISI) as a Linked Third Party of beneficiary THALIT. UNISI's contribution is 8 PMs (see Table 26) in tasks 3.4, 4.1 and 4.4. with cost of 45.000€ (see *Table 27*).

Table26. AMPERE total effort (PMs) of THALIT.

	WP1	WP2	WP3	WP4	WP5	WP6	WP7	WP8	TOTAL
PMs DoA THALIT	40	8	10	14	3	7	5	1	88
New PMs	40	8	**11**	**16**	3	7	5	1	**91**
- THALIT	40	8	**7**	**12**	3	7	5	1	**83**
- UNISI	0	0	**4**	**4**	0	0	0	0	**8**

Table 27. AMPERE total budget of THALIT.

	Direct personnel costs	Other direct costs	Direct cost of subcontracting	Indirect costs	Total
Budget DoA THALIT	396.000€	50.500€	15.000€	111.625€	573.125€
New budget	409.500€	49.000 €	0	114.625€	573.125€
- THALIT	373.500€	49.000€	0	105.625€	528.125€
- UNISI	36.000€	0	0	9.000€	45.000€

4. Modifications in description of tasks 5.3 and 5.4. Responsibility of developing the scheduling algorithms for the Linux kernel is changed from beneficiary EVI to beneficiary SSSA. In addition, EVI commits in the development of a subset of the POSIX standard. The change should better align DoA to the exploitation opportunities.
5. Deletion of contribution of TRT in the task 4.3, since TRT didn't have any PM assigned in the WP4.
6. Correction of delivery dates of D3.1. (from M36 to M6), D4.1 (from M15 to M6) and D6.1 (from M15 to M6).
7. Addition of a table which specifies work package leaders in DoA part B section 3.2

The final distribution of PMs and budget per beneficiary after the amendment are represented in Table 28 and Table 29 respectively.

Table28. Current AMPERE PMs distribution.

Beneficiary	WP1	WP2	WP3	WP4	WP5	WP6	WP7	WP8	Total
BSC	4	30	11	14	2	16	12	21	110
ISEP	2	11	28	12	0	6	2	0,5	61,5
IPP	0	1	2	0	0	0	0	0,5	3,5
ETHZ	1	4	19	16	2	8	2	1	53
SSSA	14	14	8	16	10	3	2	1	68
EVI	10	2	2	2	46	5	6	1	74
BOS	22	3	14	3	0	12	5	1	60
TRT	10	4	2	0	8	28	5	1	58
THALIT	40	8	7	12	3	7	5	1	83

UNISI	0	0	4	4	0	0	0	0	8
SYS	2	3	0	6	22	10	1	1	45
SYS GmbH	1	1	0	2	8	5	2	0	19
Total	106	81	97	87	101	100	42	29	643

Table 29. Current AMPERE budget distribution.

Beneficiary	Personnel costs	Subcontracting	Other direct costs	Indirect costs	Total Cost
BSC	495.000 €		71.000 €	141.500 €	707.500 €
ISEP	227.500 €		33.500 €	65.250 €	326.250 €
ETHZ	365.700 €		32.500 €	99.550 €	497.750 €
SSSA	340.000 €		31.500 €	92.875 €	464.375 €
EVI	370.000 €		27.000 €	99.250 €	496.250 €
BOS	382.998 €		16.500 €	99.875 €	499.373 €
TRT	547.404 €		31.500 €	144.726 €	723.630 €
THALIT	373.500 €		49.000 €	105.625 €	528.125 €
UNISI	36.000 €		0 €	9.000 €	45.000 €
SYS	324.450 €	60.000 €	53.000 €	94.363 €	531.813 €
SYS GmbH	136.990 €		6.500 €	35.873 €	179.363 €
Total	3.599.542 €	60.000 €	352.000 €	987.886 €	4.999.428 €

6.2. Delays in deliverables submission

As an unforeseen risk appeared COVID-19 outbreak which provoked different difficulties (listed in section 3.8, task 8.3) which resulted in one to three months delays in first deliverables of WP1-WP6. The delays have been timely communicated and the reasons explained to the Project Officer. It is expected that the delays will be compensated along the project course.

6.3. Deviations in resources usage

In WP8 some minor underspending of PMs of some partners has been identified. The financial report (Section 7) has been shared among all the partners, to make all aware of these deviations and if necessary to think of the way for overcoming them. They should adapt their personnel effort during the next phases of the project accordingly to the budget and the tasks assigned to them.

7. M1-M9 financial report

With a notice that part of the effort was an estimation due to the lack of this information before the end of the year/Periodic Report, we report Persons Months effort spent in each WP (Table 30 and Figure 6) and by each beneficiary (Table 31 and Figure 7) in the first nine months of the Project.

Table 30. Planned and spent AMPERE effort (PMs) per WP in the M1-M9 period of the project.

Work Package	Work Package title	Lead beneficiary	Total budget PMs	PMs initially planned to be used M1-M9	M1-M9 reported PMs	Balance	% ofPMs used in M1-M9
WP1	System model description and Use-cases	THALIT	106	25,53	18,36	87,64	17,32%
WP2	Model transformation and code generation	BSC	81	21,06	29,09	51,91	35,91%
WP3	Multi-criteria optimization	ISEP	96	19	14,17	81,83	14,76%
WP4	Run-time parallel frameworks	SSSA	85	18,59	15,54	69,46	18,28%
WP5	Operating system and parallel platforms	EVI	101	19,55	17,6	83,4	17,43%
WP6	AMPERE System Design and Computing Software Ecosystem Integration	TRT	100	13,75	12,63	87,37	12,63%
WP7	Communication, Exploitation and Dissemination	BSC	42	6,07	4,63	37,37	11,02%
WP8	Management	BSC	29	9,95	11,46	17,54	39,52%
		total	**640**	**133,5**	**123,48**	**516,52**	**19,29%**

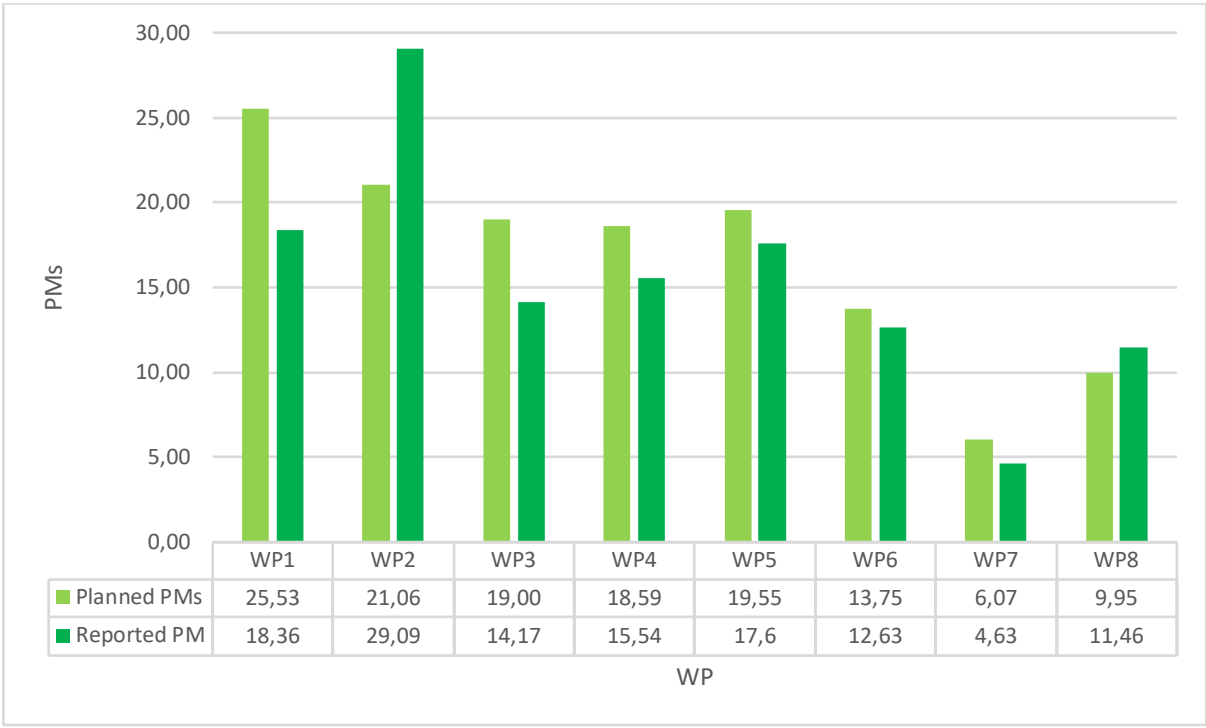

Figure 6. Planned and spent AMPERE effort (PMs) per WP in the M1-M9 period of the project.

Table 31. Planned and spent AMPERE effort (PMs) per partner in the M1-M9 period of the project.

Partner	Total budget PMs	PMs initially planned to be used M1-M9	M1-M9 reported PMs	Balance	% of PMs used in M1-M9
BSC	110	30,25	40	70	36,36%
ISEP	65	10,00	3,8	61,2	5,85%
ETHZ	53	14	14	39	26,42%
SSSA	68	13,5	16	52	23,53%
EVI	74	9,75	3,1	70,9	4,19%
BOS	60	15	15,8	44,2	26,33%
TRT	58	14	11,64	46,36	20,07%
THALIT	88	20,75	12,89	75,11	14,65%
SYS	64	16	6,25	57,75	9,77%
total	**640**	**143,25**	**123,48**	**516,52**	**19,29%**

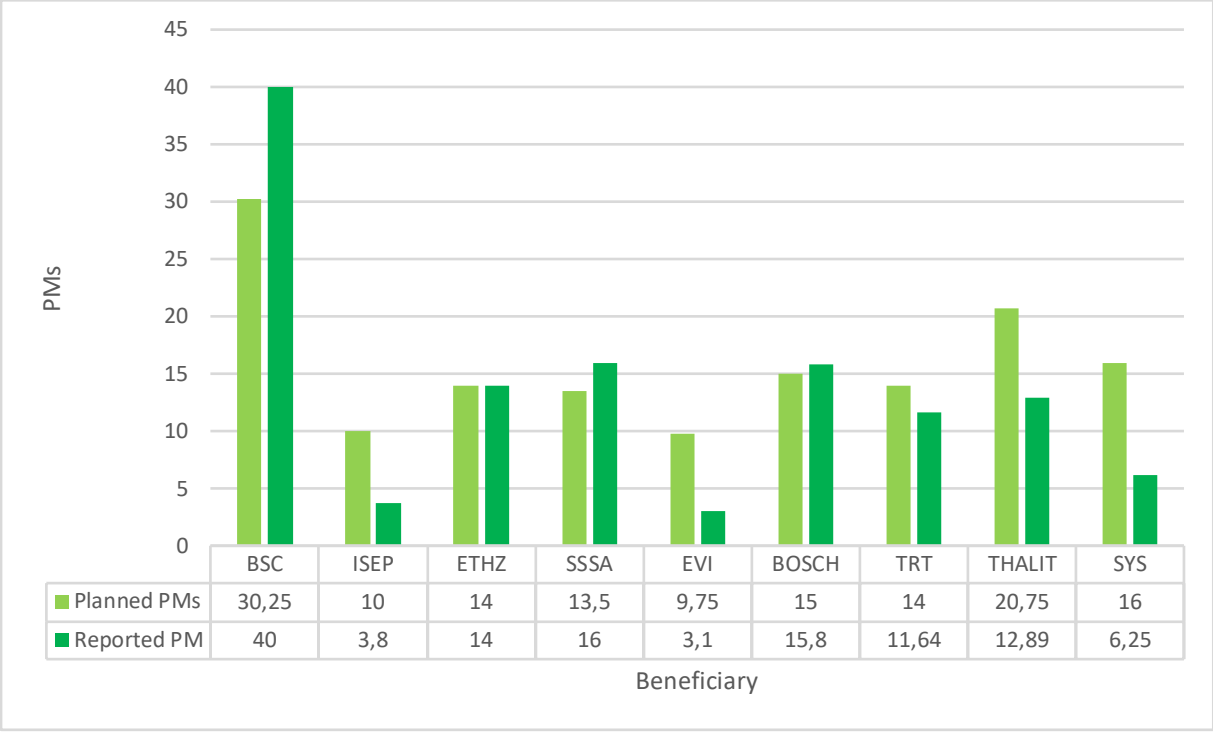

Figure 7. Planned and spent AMPERE effort (PMs) per partner in the M1-M9 period of the project.

In the first nine months period, BSC has put more effort than it would be expected for a uniform distribution of workload. In the Management WP, higher involvement is actually needed in the initial period to set-up the management tools and procedures, to negotiate the CA and prepare of all four deliverables in this WP. Maintenance of the tools and updates of the deliverables are expected to take less effort in the rest of the project. In addition, during the first months of the project, high involvement was needed in WP2 and WP6 for the following reasons:

- In case of WP2, extra effort was needed to better understand the modelling capabilities of AMALTHEA to capture the parallel opportunities exposed in the model. This has allowed BSC to better assess the suitability of the DAG as the meta-parallel programming model, and OpenMP as the primary PPM.
- In case of WP6, BSC decided to take the leadership and so extra effort was allocated to identify the interfaces among the different software components, and so avoid integration difficulties in the future.

This extra effort was already planned for Phase 2, so by the time of the first reporting period, we expect the effort to balance out.

During the first nine months of the project, ISEP has consumed 5,85% of the total effort. This percentage was mostly foreseen, knowing that the major effort of this beneficiary was planned to start in month 7 of the project, with their contribution to tasks 2.2, 2.4, 3.1, 3.2, 3.3, 4.2 and 4.3. Due to the COVID-19 outbreak, ISEP is encountering difficulties to recruit personnel specifically assigned for the project. This led to later completion of phase 1 tasks (corresponding to 2 PMs not being reported) and later onset of phase 2 tasks, (corresponding to 4 PMs not being reported). Once a researcher will be assigned, the effort expenditure is expected to be progressively increased.

Beneficiaries ETHZ, SSSA and BOS have used 26%, 24% and 26% of the total effort respectively, in line with the plan and with the budget in the DoA.

Beneficiary EVI has used 4% of available Person Months which is explained by COVID-19 outbreak that provoked issues in accessing the development environment of the project and hiring personnel dedicated to the project. In addition, the process of beneficiary's integration into Huawei which acquired EVI, took longer than expected and redirected part of the workforce on urgent integration tasks. This is however not expected to provoke delays in the future deliverables. Allocation of more personnel to the AMPERE project is foreseen starting from October, which should balance the effort expenditure.

TRT has used 20% of available personnel budget so far. Due to the COVID-19 outbreak, the organization has delayed initial contributions in the Work Package 6 until the beginning of September which is reflected in the lower use of resources.

COVID-19 outbreak has also affected internal recruitment process for the project of the beneficiary THALIT which slowed down WP1 activities. Due to suspension of work and forced leaves requested by company to mitigate the financial impact of lockdown, the use of resources was reduced in comparison to the initial estimation. The following table reports the detailed difference, where it can be seen that the impact was particularly heavy on April and May when the Italian National lockdown was fully activated and company requested to employees to spend one, two days a week (in average) on holidays. Regardless of the real activity implemented by engineers, the effort that could be reported decreased. Nevertheless, all the activities related to T1.1 were done and the initial activities associated to T1.2, T1.3 and T1.4 will be recovered in Phase 2.

	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	TOTAL
PM reported	0,84	1,30	1,59	1,27	1,31	1,62	1,88	0,84	2,23	12,87
PM estimated	0,75	1,5	3,5	3,5	3,5	3	3	1	1	20,75
Difference	-0,09	0,20	1,91	2,23	2,19	1,38	1,12	0,16	-1,23	7,88

Personnel is eventually recruited and the initial underspending (15% of available budget for personnel has been used by now) is being progressively recovered now.

SYS has used 6,25 PMs out of 16 PMs initially planned to be used in the first nine months of the project. This happened because of internal restructuring of resources in SYS which resulted in the need to involve its Third Party, SYS GmbH, in the project. SYS GmbH was contributing to the implementation of AMPERE tasks since the beginning of the project, but it was included as SYS's Third Party in month 6 with the first project amendment. In this way its initial effort was not reported. Additionally, due to COVID-19 outbreak, SYSGO GmbH made reduction of working hours of the personnel from five to four days per week which also

resulted in reporting less effort than initially foreseen. This jointly is reflected in use of 10% of total available Person Months of the beneficiary so far. All tasks in which SYS was initially planned to participate in first nine months of the project have been achieved, with an exception of accomplishment of the task 7.2 Exploitation activities, which is still on-going.

It is expected that all partners will make effort to adapt their personnel effort during the forthcoming period in the project accordingly to the budget and the tasks assigned to them.

8. Acronyms

ACRONYM	
ACC	Adaptive Cruise Control
AI	Artificial Intelligence
AMPERE	A Model-driven development framework for highly Parallel and EneRgy-Efficient computation supporting multi-criteria optimisation
API	Application Programming Interface
BSC	Barcelona Supercomputing Center - Centro Nacional de Supercomputacion
BOS	Bosch
CA	Consortium Agreement
CPS	Cyber Physical System
CPSoS	Cyber-Physical Systems of Systems
DNN	Deep Neural Network
DoA	Description of Action
DSML	Domain Specific Modelling Language
EAS	Energy-Aware Scheduling
ETHZ	Eidgenössische Technische Hochschule Zürich
EVI	Evidence S.r.l.
FPGA	Field Programmable Gate Array
IPR	Intellectual Property Rights
ISEP	Instituto Superior de Engenharia do Porto
KPI	Key Performance Indicator
NFR	Non Functional Requirement
ODAS	Obstacle Detection and Avoidance System